MEMORY DATABOOK 1983



JK SEMICONDUCT

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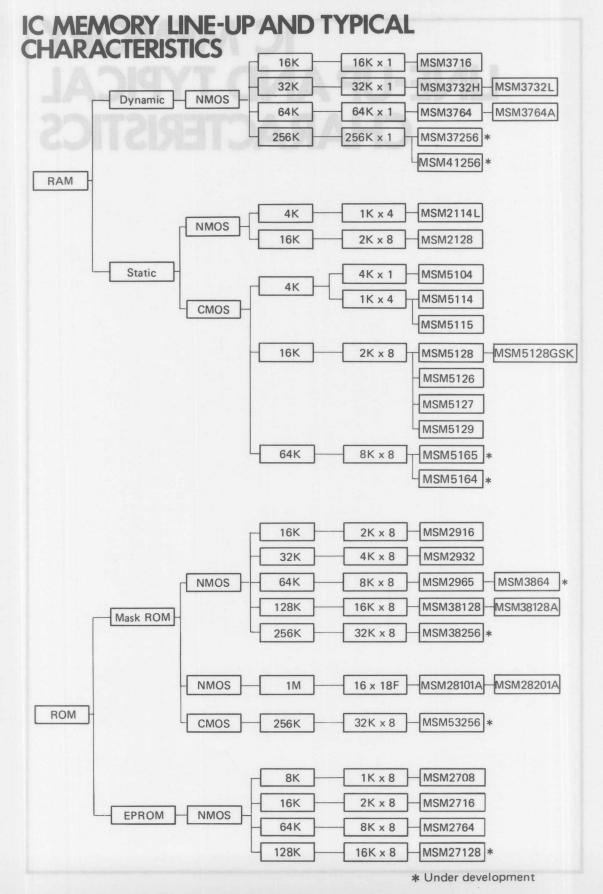
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• DYNAMIC RAMS

Model Name	Mem- ory Capac- ity	Circuit Function	Memory Configura- tion	Num- ber of Pins per Pack- age	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consump- tion MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM3716-2	401	10.0: 0	10.004 4	40	150	375	528/20	+12,+5	MK4116-2
MSM3716-3	16k	16 Pin Dynamic	16,384 x 1	16	200	375	528/20	-5	MK4116-3
MSM3732H-15	32k	16 Pin Dynamic	22.7601	16	150	270	248/28		S-81 (9142)
MSM3732H-20	32K	A7 (Column)=H	32,768 x 1	16	200	330	248/28	+5	2-0-11/2/11/04
MSM3732L-15	32k	16 Pin Dynamic	32,768 x 1	16	150	270	248/28		A BOX FOR CO.
MSM3732L-20	32K	A7 (Column)= L	32,700 X T	10	200	330	248/28	+5	ISMB104-2
MSM3764-15	CAL	10 P: P	05 500 4	40	150	270	248/28		TMS4164-15
MSM3764-20	64k	16 Pin Dynamic	65,536 x 1	16	200	330	248/28	+5	TMS4164-20
MSM3764A-12		ve otace ooc	007		120	230	330/28		0C-85 18M26
MSM3764A-15	64K	16 Pin Dynamic	65,536 x 1	16	150	260	330/28	+5	
MSM3764A-20	3+	180 30010.27	Uni	5 8	200	330	330/28	16K	at-42 tawas
MSM37256-15		15.0(015 005	1005		150	270	440/28	201	USPAR FEMAR
MSM37256-20	256k	16 Pin Dynamic	262,144×1	16	200	330	440/28	+5	91-60 (3M8)
MSM41256-10					100	200	415/28	- 100	00 00 17100
MSM41256-12	256k	16 Pin Dynamic	262,144×1	1 16	120	230	415/28	+5	ISM6126-20
MSM41256-15		201,01686 . 005	200		150	280	415/28	1610	as as tamen

• NMOS STATIC RAMS

Model Name	Mem- ory Capac- ity	Circuit Function	Memory Configura- tion	Num- ber of Pins per Pack- age	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2114L-2	12,+6	450 800	24 450	83	200	200	396	ив	2114L2
MSM2114L-3	4K	Static, Common I/O	1024 × 4	18	300	300	396	+5	2114L3
MSM2114L	8+	200 790/188	005 85	82	450	450	396	SAR	2114L
MSM2128-12	24	280 288/184	18 280	Bul	120	120	660/110	128k	BOLCOMS
MSM2128-15	16K	Static, Common I/O with Power Down Mode	2048 × 8	24	150	150	550/110	+5	TMM2016 M58725
MSM2128-20					200	200	550/110		

■IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

• CMOS STATIC RAMS

Model Name	Mem- ory Capac- ity	Circuit Function	Memory Configura- tion	Num- ber of Pins per Pack- age	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consump- tion MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM5114-2		Standby			200	200	192/0.04		
MSM5114-3	4K	Fully Static, Common I/O	1024×4	18	300	300	192/0.04	+5	TC5514 µPD444
MSM5114	3-	978	200		450	450	192/0.04		MSM3716-37
MSM5115-2	46	Clocked Static,	1001	1 1 2	200	300	33/0.04	32k	
MSM5115-3	4K	Common I/O	1024×4	18	300	420	33/0.04	+5	HM6514
MSM5104-2	24	Clocked Static.	001	1 11	200	300	33/0.04	32k	
MSM5104-3	4K	Common I/O	4096×1	18	300	420	33/0.04	+5	HM6504
MSM5128-12	-8+	621892 077	1001	r fa	120	120	330/0.275	Bilk	CHECKER
MSM5128-15	16K	Fully Static, Common I/O	2048×8	24	150	150	300/0.275	+5	HM6116 µPD446
MSM5128-20		83/068 7 7 88	120		200	200	275/0.275		CALL TO THE REAL PROPERTY OF THE PARTY OF TH
MSM5127-15	16K	Fully Static	001		150	150	300/0.275	2010	21-PAPEN SIVIGI
MSM5127-20	16K	Common I/O	2048×8	24	200	200	275/0.275	+5	
MSM5129-15	16K	Fully Static	001	t Ix	150	150	300/0.275	+5	UT-COST CATOR
MSM5129-20	16K	Common I/O	2048×8	24	200	200	275/0.275	+5	
MSM5126-20	16K	Fully Static	2040 6	0.4	150	150	385/0.165		UI GUSTANICA
MSM5126-25	16K	Common I/O	2048×8	24	200	200	385/0.165	+5	
		03/077 020	981		100	100			01-002126408
MSM5165	64K	Fully Static Common I/O	8192x8	28	120	120	495/5.5	+5	
					150	150			

EPROMS

Model Name	Mem- ory Capac- ity	Circuit Function	Memory Configura- tion	Num- ber of Pins per Pack- age	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consump- tion MAX (mW) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2708	8k	24 Pin EPROM	1024 x 8	24	450	450	800	+12,+5 -5	2708
MSM2716	16k	24 Pin EPROM	2048 x 8	24	450	450	525/132	+5	2716
MSM2764	64k	28 Pin EPROM	8192×8	28	200	200	790/185	+5	2764
MSM27128	128k	28 Pin EPROM	16,384x8	28	250	250	788/184	+5	27128

• MASK ROMS

Model Name	Mem- ory Capac- ity	Circuit Function	Memory Configura- tion	Num- ber of Pins per Pack- age	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consump- tion MAX (mW) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2916	16K	24 Pin MASK ROM	2048x8	24	250	250	550	+5	2716 EPROM
MSM2932	32K	24 Pin MASK ROM	4096x8	24	300	300	687	+5	2532 EPROM
MSM2965	64K	24 Pin MASK ROM	8192×8	24	300	300	687	+5	
MSM3864	64K	28 Pin MASK ROM	8192×8	28	250	250	550	+5	
MSM38128	128K	28 Pin MASK ROM	16384x8	28	450	450	660/110	+5	
MSM38128A	128K	28 Pin MASK ROM	16384x8	28	250	250	550	+5	
MSM38256	256K	28 Pin MASK ROM	32768x8	28	250	250	660	+5	
MSM28101		40 Pin MASK RAM	3760×16	40	40.0	00.0	000		JIS-Chinese- character coding system 0~7, 16~47
MSM28201	1M	18x16 Chinese-cha- racter font output	x18	40	10μS	22μS	893	+5	JIS Chinese- character coding system 48~87
MSM53256	256K	28 Pin CMOS MASK ROM	32768×8	28	200	200		+5	

. MASK ROMS

2

PACKAGING

lots: Model names suffixed by RS denote plastic mold devices, while AS denotes cerdip or side-brazed devices

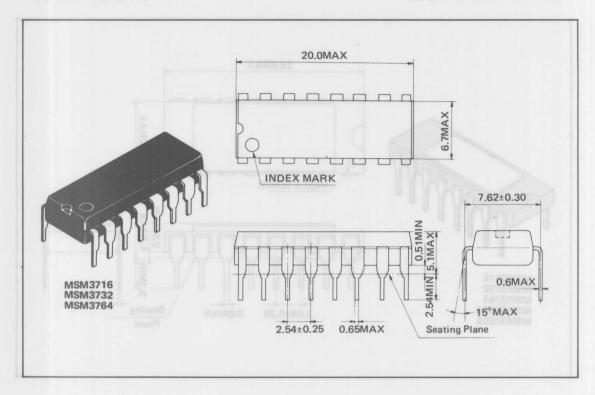
		Pack	ages	
Name	No. of Pins	RS		AS
	No. of Filis	PLASTIC	CERDIP	SIDE-BRAZED
MSM3716	16	0		0
3732	16	0		0
3764	16	0		0
3764A	16	0		0
37256	16			0
2114L	18	0		0
2128	24	0		
5104	18	0		0
5114	18	0		0
5115	18	0		0
5126	24	0		
5127	24	0		
5128	24	0		
5129	24	0		
5165	28	0		0
2916	24	0	0	
2932	24	0	0	
2965	24	0		
3864	28	0		
38128	28	0		
38128A	28	0		
38256	28	0 .		
38256A	28	0		
53256	28	0		
28101A	40			0
28201A	40			0
2708	24		0	
2716	24		0	
2764	28		0	
27128	28		0	

Note: Model names suffixed by RS denote plastic mold devices, while AS denotes cerdip or side-brazed devices.

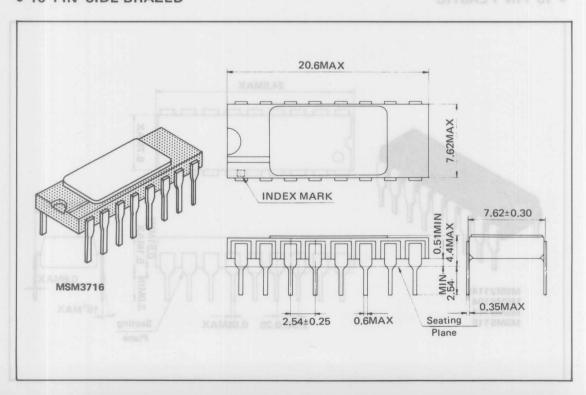
Ex. MSM2916RS..... plastic mold device

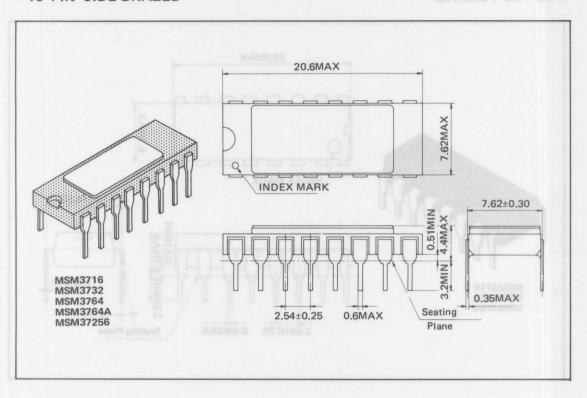
MSM2916AS..... cerdip or side-brazed device

• 16 PIN PLASTIC

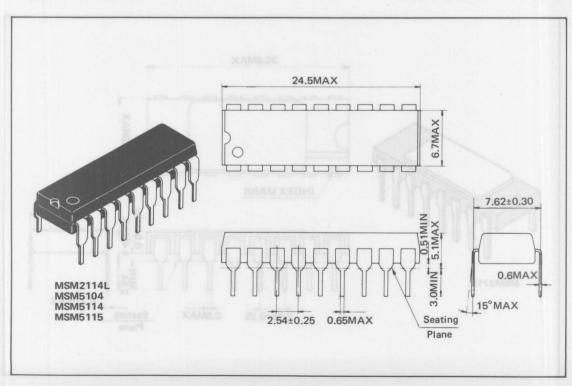


• 16 PIN SIDE-BRAZED

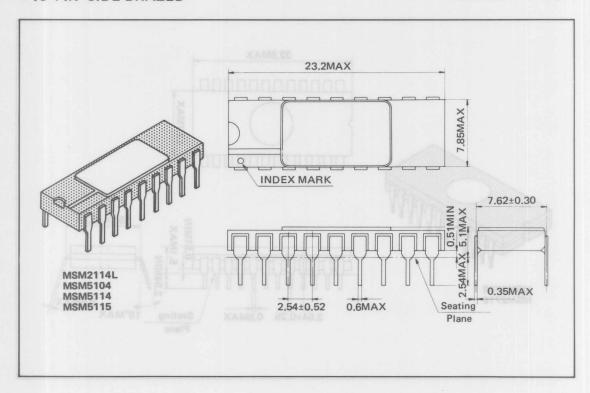




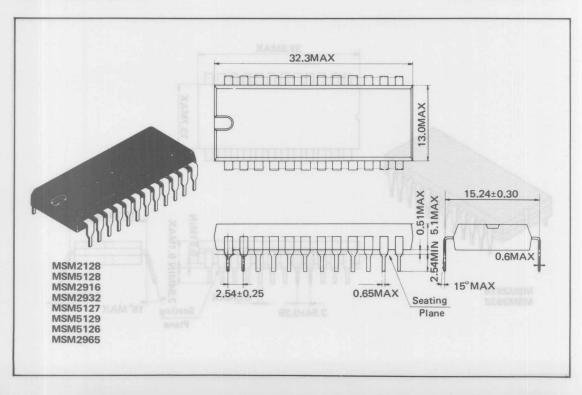
• 18 PIN PLASTIC

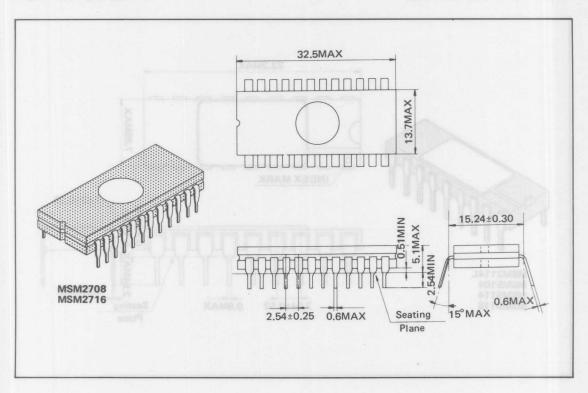


• 18 PIN SIDE-BRAZED

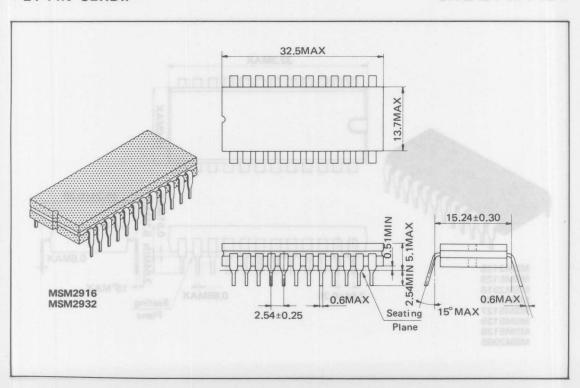


• 24 PIN PLASTIC

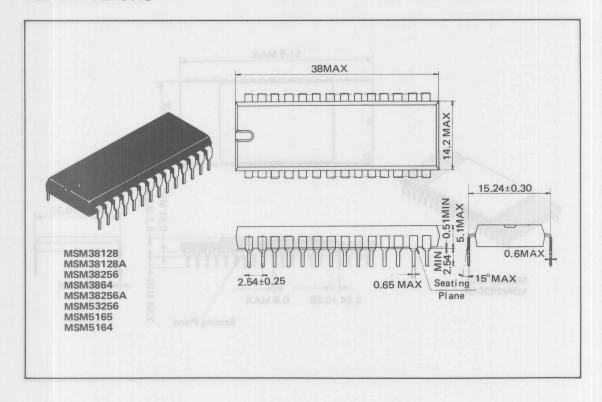




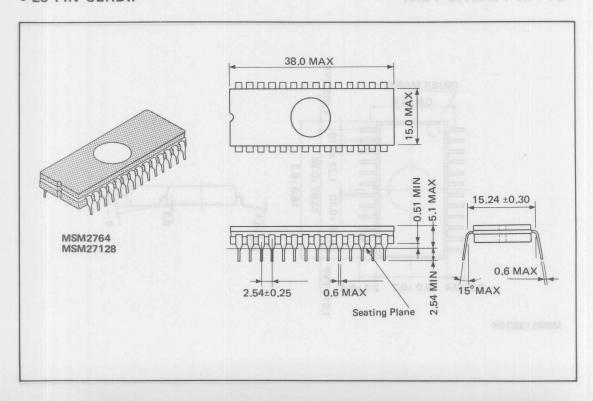
• 24 PIN CERDIP

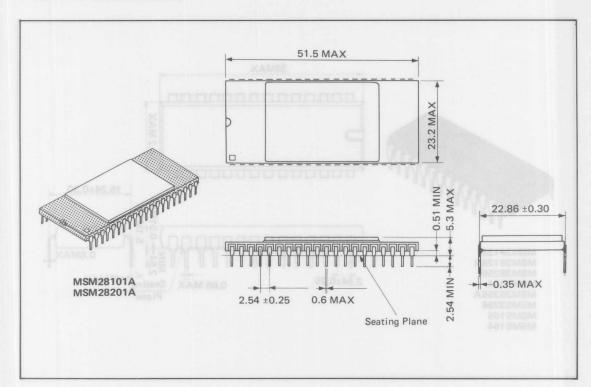


• 28 PIN PLASTIC

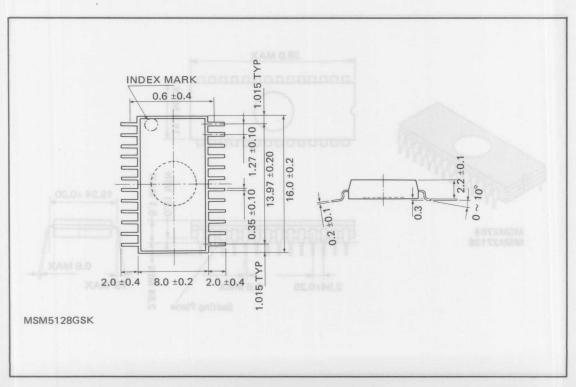


• 28 PIN CERDIP





• 24 PIN PLASTIC FLAT



RELIABILITY

explosive progress of semiconductor technology. They use some of the most advanced design and manuscriming rechnology developed so date. With greater negligation, diversity and reliability, their applications leve expended enormously. Their use in large scale computers, control equipment, calculators, electronic lames and in many other fields has increased at a fest

h failure in efectionic banking or telaphone switching quipment, for exemple, could have far reaching effects nd can cause incalculable losses. So, the demand, for table high quality mamory devices is strong.

(a) at Oki Electric is fully aware of this damand. So to have adopted a comprehensive quality assurance vitem based on the concept of consistency in development, mention and cales.

With the increasing demand for improvement in function, capability and reliability, we will expend our efforts in the future. Our quality insurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

he quality assurance system employed by Oki Electric on be divided into a major stages: device planning, evelopmental prototype, production prototype, and has production. This system is outlined in the followng block diagram (Fig. 1-1).

Dovice planning stage

o manufacture devices that meet the market demands no satisfy continner needs, we carefully consider unctional and failure rate requirements, utilization out, environment and other conditions. Once we etermine the proper type, material and structure, so chack the design and manufacturing techniques and he line processing capacity. Then we prepare the explanation and time etherline.

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We determine circuits, pattern design, process settings, seambly techniques and structural requirements during this stage. At the same time, we carry out actual proto-

ince device quality is largely determined during the estimation (10 file fleetric pays careful attention to unity confirmation during this steen.

now we do it:

Les completion of circuit design for parter
casign), personnal from the design, process even
notagy, production technology, installation sech
notagy and reliability departments per together for
a thorough review to ansure design quality and to
anticipate problems that may occur during may
production. Past experience and know now guide
three discussions.

Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.

Note: TEG (Test Elament Group) refers to the device group designed for stability evaluation of MOS transistors, clodes, resistors and other circuit component alement used in USI memories.

(3) Prototypes are subjected to repeated reliability one other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Praduction prototype stage

During this stage, various tests check the reliability and other special features of the production prototype a the mais production factory level. After confirming the quality of device, we prepare the various standard the quality of device, we prepare the various standard required for mass production, and then start production on the reduction prototype are much the same a those performed on the developmental prototype, the personnel, facilities and production sits differ for the two prototypes, independent prototypes, and production sits differ for the

4) Mass production
During the mass production stage, careful management
of purchased materials, parts and facilities used during
the manufacturing process, measuring equipment
manufacturing conditions and environment is receivant
to ensure device quality first stipulated during th
designing stages. The manufacturing process finduction
inspection of the completed device) is followed by a lor
impection of the completed device) is followed by a lor
guitantee inspection to chook that the specified quality
is maintained under conditions identical to those under
which a customer would actually use the device. This
lot guerance inspection is parformed in 3 ciffurant
forms as shown helpsy.

1. INTRODUCTION

Semiconductor memories play a leading role in the explosive progress of semiconductor technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

RELIABILITY INFORMATION

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable high quality memory devices is strong.

We, at Oki Electric is fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki Electric can be divided into 4 major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1-1).

1) Device planning stage

To manufacture devices that meet the market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing.

Since device quality is largely determined during the designing stage, Oki Electric pays careful attention to quality confirmation during this stage.

This is how we do it:

- (1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.
- (2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.

Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

(3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in 3 different forms as shown below.

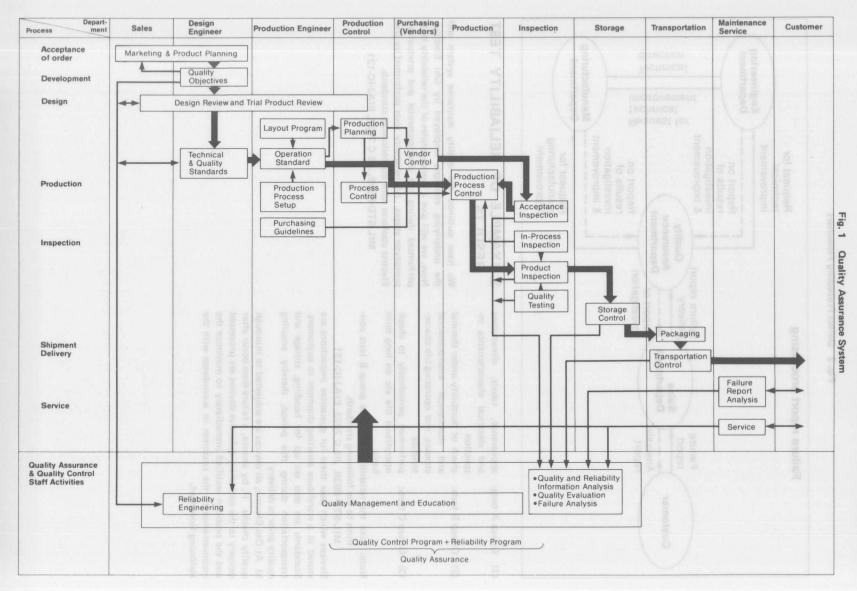
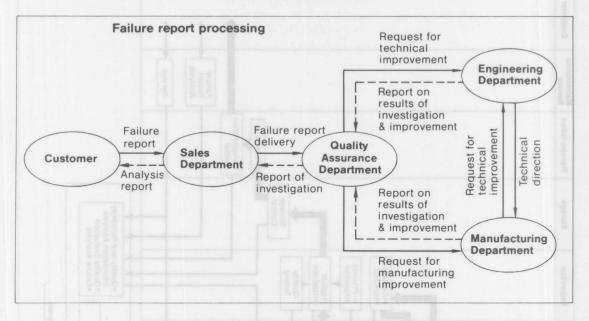


Fig. 2 Defect Processing Flowchart



(1) Group A tests: appearance, labels, dimensions

and electrical characteristics inspection

(2) Group B tests:

check of durability under thermal and mechanical environmental stresses, and operating life characteristics

(3) Group C tests:

performed periodically to check operational life etc on long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery.

5) At Oki Electric, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

3. EXAMPLE OF RELIABILITY TEST RESULTS

We have outlined the quality assurance system and the underlying concepts employed by Oki Electric. Now, we will give a few examples of the reliability tests performed during the developmental and production prototype stages. All reliability tests performed by Oki Electric conform with the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

OKI MEMORY LSI LIFE TEST RESULTS

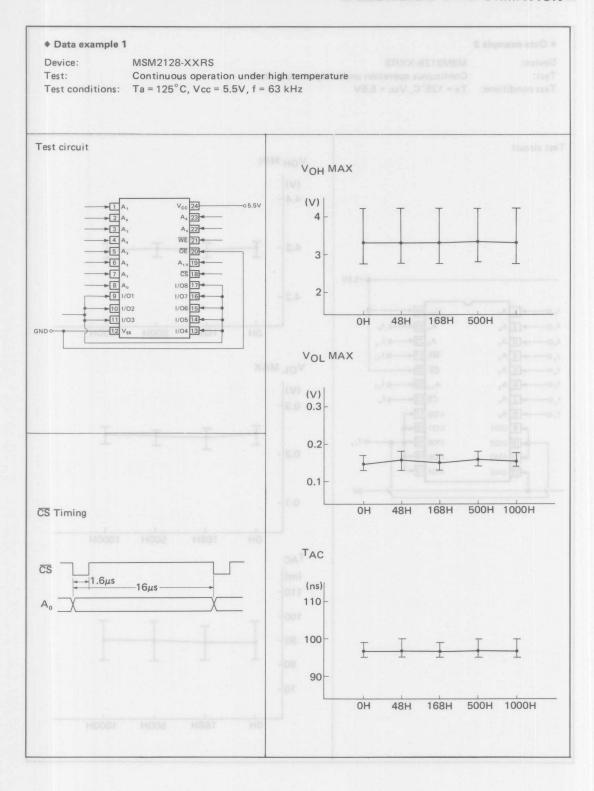
	Device name	MSM3764-XXRS		MSM2128-XXRS			MSM5128-XXRS			
Function		65536 x 1 bit DYNAMIC RAM Si gate N-MOS 16P plastic package			2048 x 8 bit STATIC RAM Si gate N-MOS 24P plastic package			2048 x 8 bit STATIC RAM Si gate C-MOS 24P plastic package		
Operating life test	Ta = 125°C Vcc = 5.5V	175	3000	0	40	1000	0	100	1000	0
	Ta = 150°C Vcc = 5.5V	50	1000	0	100 oyd 104a~20	1	elder	50	2000	0
Temperature humidity test	140°C 85% Vcc = 5.5V	90	100	0	X ni sam	1 1	yansu	20	100	0
	85°C 85% Vcc = 5.5V	520	3000	0	40	1000	0	70	1000	0
Pressure cooker test	121°C 100% No bias	340	300	0	40	300	0	50	300	0

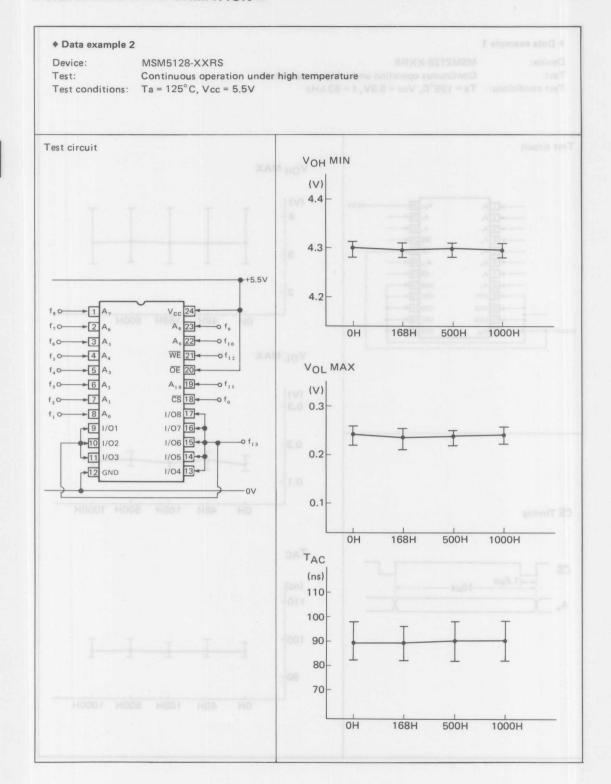
	Device name			MSM2764-AS			MSM38128-XXRS			MSM2965-XXRS		
	Function		192 x 8 asable E	bit P ROM	16384 x 8 bi Mask ROM			8192 x Mask R				
	Structure	Si gate N-MOS 28 P cerdip			Si gate N-MOS 28P plastic package			Si gate N-MOS 24P plastic package				
Test item	Test condition	Sample size	Test hours	Failures	Sample Size	Test hours	Failures	Sample	Test hours	Failure		
Operating life test	Ta = 125°C Vcc = 5.5V	0	na .	2	40	2000	0	40	2000	0		
	Ta = 150°C Vcc = 5.5V	40	1000	0	10 eyol		Nock		lamo	ert.		
Temperature humidity test	140°C 85% Vcc = 5.5V		(-65°-	150°C	-TRI-O	88-			77	92		
	85° C 85% Vcc = 5.5V	50	1000	0	20	2000	0	40	1500	0		
Pressure cooker test	121° C 100% No bias		20=1	euro	40	500	0	40	168	0		
			68	4 min per cycle 4 times in X, Y, Z		frequency vibration						

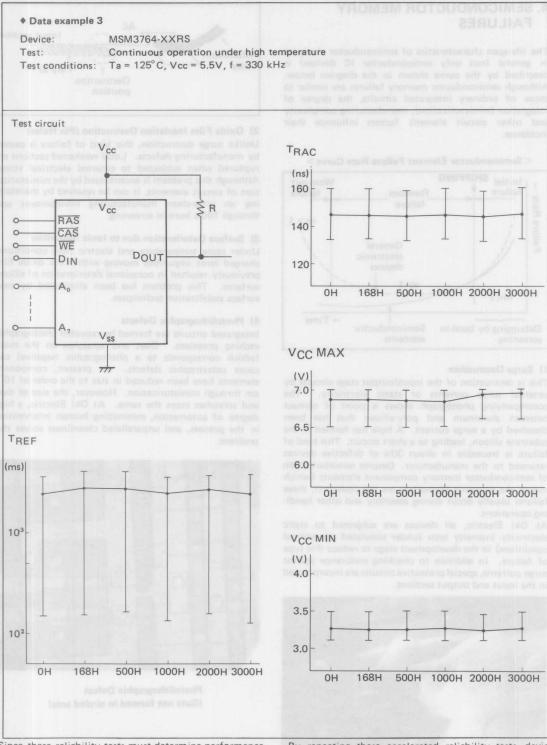
OKI MEMORY LSI ENVIRONMENTAL TEST RESULTS

Device name Test item Test condition				64-XXRS	MSM212	28-XXRS	MSM5128-XXRS	
				Failures	Sample size	Failures	Sample size	Failures
gate C-MÖS plastic package	Soldering heat	260° C 10 sec	20	0	20	8 0	25	0
Thermal environmental	Thermal shock	0°C~100°C 5 min 5 min 10 cycles	faeT- a	Common St.	oltibuos		25	
test	Temperature cycling	-55° C~RT~150° C 30 min 30 min 100 cycles	320	0	100	0	65	0
0 0007	Variable	100Hz~200Hz	UUUT	00	- Va.a -	paV		
	frequency vibration	4 min per cycle 4 times in X, Y, Z	001	00	C 85%	140°	-	
Mechanical environmental test	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z	20	0	20	0	18	0
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z	300	340	10039 bist	N ISI	701	Proteorer s
Electrical Environmental test	ESD	200pF, 0Ω, 5 times	10	0	10	0	10	0

Test item		Device name	MSM2	2764AS	MSM381	28-XXRS	MSM2965-XXRS	
		Test condition	Sample size	Failures	Sample size	Failures	Sample size	Failures
hours Fallure	Soldering heat	260° C 10 sec	smoul exis		holisbado	1807	moti	901
2000 0	Thermal shock	0° C~100° C 5 min 5 min 10 cycles	50	0	10	Vec	50	Operation
Thermal environmental test	Temperature cycling	-55° C~RT~150° C 30 min 30 min 100 cycles	50 (-65°~ RT~ 150°C 30′3′ 30′	0	126	0	80	0
n gar	08 0	40 500	20∞)		100%	121		81023519
	Variable frequency vibration	100Hz~200Hz 4 min per cycle 4 times in X, Y, Z			88183			181000
Mechanical environmental test	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z	50	0				
	Constant 10000G or 20000G acceleration 1 min in each X, Y, Z							
Electrical environmental test	ESD	200pF, 0Ω, 5 times	10	0	10	0	10	0







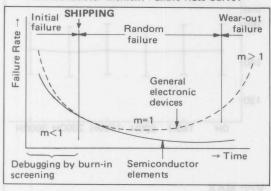
Since these reliability tests must determine performance under actual working conditions in a short period of time, they are performed under severe test conditions. For example, the 125° C high temperature continuous operation test performed for 1000 hours is equivalent to testing device life from 2 to 300 years of use at Ta = 40° C.

By repeating these accelerated reliability tests, device quality is checked and defects analyzed. The resulting information is extremely useful in improving the manufacturing processes. Some of the more common defects in memory LSI elements and their analysis are described below.

4. SEMICONDUCTOR MEMORY FAILURES

The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) is described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.

< Semiconductor Element Failure Rate Curve >



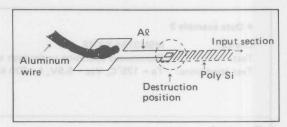
1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and poly-silicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations.

At Oki Electric, all devices are subjected to static electricity intensity tests (under simulated operational conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.



Example of surge destruction



2) Oxide Film Insulation Destruction (Pin Holes)

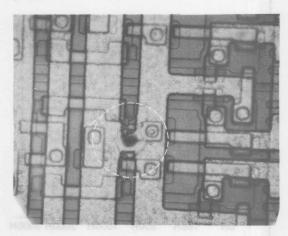
Unlike surge destruction, this kind of failure is caused by manufacturing defects. Local weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

3) Surface Deterioration due to Ionic Impurities

Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10^{-4} cm through miniaturization. However, the size of dust and scratches stays the same. At Oki Electric, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness solves this problem.



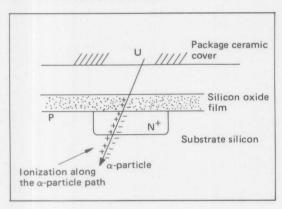
Photolithographic Defect (Gate not formed in circled area)

5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki Electric has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

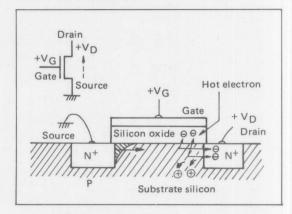
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 64-kilobit RAMs. The inversion of memory cell data by alpha-particle generated by radioactive elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki Electric we have eliminated the problem by coating the chip surface of 64-kilobit RAMs with a resin which effectively screens out these alpha-particle.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5 V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electron

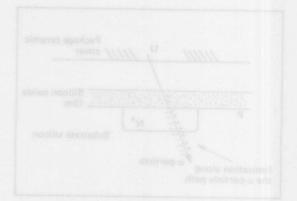
With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, we at Oki Electric have been continually improving our production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

5) Aluminum Corrector

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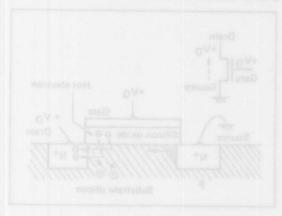
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MOS MEMORY HANDLING PRECAUTIONS

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Idresses from other driver boards, it is highly

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- 3) Methods available for eliminating undershooting generated in the address line include
- Samping of the undershooting by includingliade.
- b) Connect 10~200 in safes with driver outputs,
 c) Smooth the rising edge and falling edge wave
 - 3. CMOS Memory Operating Procautions

3.1 Lateh-Up

If the CMOS memory input signal level exceeds the vice power line voltage by +0.3 V, or drops below the ground potential by -0.3 V, the latch-up mechanism may be activated. And once this latch-up mode he been equivated, the memory power has to be switched off before normal operating mode can be restored Destruction of the memory element is also possible if the power is not switched off.

Although OH: CMOS memories have been designed to counter these tendencies, it is still recommended that input signal overshooting and undershooting by avoided

3.2 Battery Badic-Up

Take apecial note of the following 4 points when designing battery back-up systems.

If Do not permit the input signal H level to exceed Voc +0.3 V when the memory Vcc power is dropped To echieve this, it is recommended that a CMDS driver using a Vcc power common with the CMDS memory, or an open collector buffer or open drain buffer pulled-up by a Vcc power common with the CMDS memory be used for driving purposes.

(2) Set the chip sclect input signal CE to the same Hevel as the CMOS memory Vac power line. And it order to minimize memory power consumption, set the write enable input WE level, the address input and the deta input to either ground level or to the same H level as the CMOS memory Vac power line (3) Make sure that the CMOS memory Vac power line increased without "ringing" or temporary breaks

(4) When using synchronous type CMOS memories (MSM5115, MSM5104), make sure that eccepting occurs after elapse of the chip enable off time (fcc) prescribed in the catalog after the Vcc power line has reached the guaranteed operating voltage range. For further datalis, refer to "CMOS Memory Sattery

Back-up" at the end of this manual.

Although Old MOS memories incorporate built-in corector circuits to protect all input terminals from soil destruction, it is not considered possible to give complete protection against heat destruction due to vercurrents and insulation film destruction due to require filgh voltages. It is, therefore, necessary to borrer the following precentionary measures.

Under no circumstances must voltages or currents in excess of the specified ratings be explied to any input terminal.

2) Always use an electrically conductive mat or shipoling turies for storage and transporting gurposes.

Avoid wearing apparel made of synthetic fiber during operations. The wearing of cottons which do not readily generate static electricity is desirable. Also evoid handling devices with bare hands. If handling with bere hands cannot be avoided, make sure that the body is grounded, and that a fMIT resistor is always connected between the body and ground in order to prevent the generation of static electricity.

Maintaining the relative humidity in the operation room at 50% helps to prevent static electricity. This should be remembered especially sturing dry ceasins.

When eating a soldgring loan, the iron should be prounded from the tip. And as far as possible, use loss posses soldering irons (12 V or 24 V irons).

Power Supply and Imput Signal Moles

1. Power supply notes absorbtion

In dynamic memories, the flow of power supply urrent differs greatly between accessing and standby order.

Although very little power is consumed by CMOS nemories during standby mode, considerable current drawn for charging and discharging (instantaneous drawn requirements) during access mode. In order to booth the "apike noise" generated by these current requirements, the use of relatively large capacitance apacitors (about one IQUE capacitor for every 8 to use sy response capacitors of about 0 luff for each usercy response capacitors of about 0 luff for each common at the second standard with a little line common at a possible is also desirable.

.2 Logot signal noise absorption

Overthirding and understooting of the input signal bould be kept to a bare minimum. Understooting it bettertals can result in loss of cell data stability within he memory. For this reason,

MOS MEMORY HANDLING PRECAUTIONS

1. Static Electricity Countermeasures

Since voltage is generally controlled by means of the transistor gate oxide film in MOS memories, the input impedance is high and the insulation tends to be destroyed more readily by static electricity.

Although Oki MOS memories incorporate built-in protector circuits to protect all input terminals from such destruction, it is not considered possible to give complete protection against heat destruction due to overcurrents and insulation film destruction due to irregular high voltages. It is, therefore, necessary to observe the following precautionary measures.

- 1) Under no circumstances must voltages or currents in excess of the specified ratings be applied to any input terminal.
- 2) Always use an electrically conductive mat or shipping tubes for storage and transporting purposes.
- 3) Avoid wearing apparel made of synthetic fiber during operations. The wearing of cottons which do not readily generate static electricity is desirable. Also avoid handling devices with bare hands. If handling with bare hands cannot be avoided, make sure that the body is grounded, and that a $1M\Omega$ resistor is always connected between the body and ground in order to prevent the generation of static
- 4) Maintaining the relative humidity in the operation room at 50% helps to prevent static electricity. This should be remembered especially during dry seasons.
- 5) When using a soldering iron, the iron should be grounded from the tip. And as far as possible, use low power soldering irons (12 V or 24 V irons).

2. Power Supply and Input Signal Noise

2.1 Power supply noise absorption

In dynamic memories, the flow of power supply current differs greatly between accessing and standby modes.

Although very little power is consumed by CMOS memories during standby mode, considerable current is drawn for charging and discharging (instantaneous current requirements) during access mode. In order to absorb the "spike noise" generated by these current requirements, the use of relatively large capacitance capacitors (about one 10µF capacitor for every 8 to 10 RAMs) is recommended along with good high frequency response capacitors of about 0.1 µF for each memory element. Power line wiring with as little line impedance as possible is also desirable.

2.2 Input signal noise absorption

Overshooting and undershooting of the input signal should be kept to a bare minimum. Undershooting in particular can result in loss of cell data stability within the memory. For this reason,

- (1) Avoid excessive undershooting when using an address common bus for memory board RAMs and
- (2) Since noise can be generated very easily when using direct drive for applying memory board RAM addresses from other driver boards, it is highly recommended that these addresses be first received by buffer.
- (3) Methods available for eliminating undershooting generated in the address line include
 - a) Clamping of the undershooting by including a diode.
 - b) Connect $10 \sim 20\Omega$ in series with driver outputs.
 - c) Smooth the rising edge and falling edge waveforms.

3. CMOS Memory Operating Precautions

3.1 Latch-Up

If the CMOS memory input signal level exceeds the Vcc power line voltage by +0.3 V, or drops below the ground potential by -0.3 V, the latch-up mechanism may be activated. And once this latch-up mode has been activated, the memory power has to be switched off before normal operating mode can be restored. Destruction of the memory element is also possible if the power is not switched off.

Although Oki CMOS memories have been designed to counter these tendencies, it is still recommended that input signal overshooting and undershooting by avoided.

3.2 Battery Back-Up

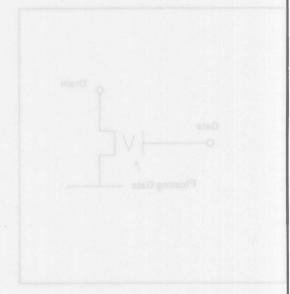
Take special note of the following 4 points when designing battery back-up systems.

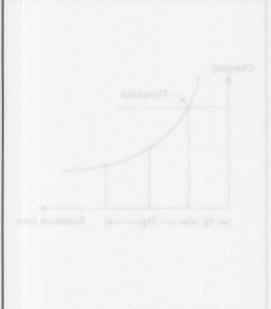
- (1) Do not permit the input signal H level to exceed Vcc +0.3 V when the memory Vcc power is dropped. To achieve this, it is recommended that a CMOS driver using a Vcc power common with the CMOS memory, or an open collector buffer or open drain buffer pulled-up by a Vcc power common with the CMOS memory be used for driving purposes.
- (2) Set the chip select input signal CE to the same H level as the CMOS memory Vcc power line. And in order to minimize memory power consumption, set the write enable input WE level, the address input and the data input to either ground level or to the same H level as the CMOS memory Vcc power line.
- (3) Make sure that the CMOS memory Vcc power line is increased without "ringing" or temporary breaks when restoring the battery back-up mode.
- (4) When using synchronous type CMOS memories (MSM5115, MSM5104), make sure that accessing occurs after elapse of the chip enable off time (tcc) prescribed in the catalog after the Vcc power line has reached the guaranteed operating voltage range. For further details, refer to "CMOS Memory Battery

Back-up" at the end of this manual.

EPROM WRITING AND

ERASURE



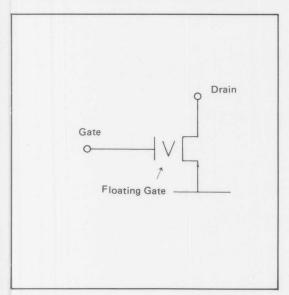


EPROM WRITING AND ERASURE

1. EPROM Writing Erasure

1.1 EPROM MSM2716/2764 writing

Writing in the MSM2716AS involves setting the drain and gate voltages of the floating gate stage to a high voltage. When the drain voltage exceeds 15 V and the gate voltage 20 V, the channel charge (electrons) becomes highly energized and flow over the oxide film barrier into the floating gate. And since the high gate voltage is positive polarity, electrons will flow into the floating gate very easily. When electrons build up in the floating gate, the memory element "threshold voltage" is changed, and subsequently stored as memory data. Once the charge has been built up, the surrounding oxide film (high insulation) prevents escape of electrons. The data is thus stored as "non-volatile" data.



When the MSM2716AS is shipped from the factory, the floating gate is left in discharged status (all bits "1"), i.e. "blank" status. During writing processes, $+25\,\mathrm{V}$ is applied to the Vpp terminal and V_{IH} to the $\overline{\mathrm{OE}}$ input. The data to be programmed is applied in parallel to the outputs (O $_0$ -7). After the address and data have been set up, application of V_{IH} level for 50 ms to the $\overline{\mathrm{CE}}$ input will enable writing of data. Since the $+25\,\mathrm{V}$ applied to Vpp is fairly close to the element's withstanding voltage, make sure that the voltage setting is maintained strictly within the $25\,\mathrm{V}$ ±1 V range. Application of voltages in excess of the rated voltage, and overshooting, to the Vpp terminal can result in permanent damage to the element.

Although MSM2716AS rewriting should be checked about 100 times by sample testing, in actual practice 5 to 10 times is usually the limit. This will not likely result in any problem.

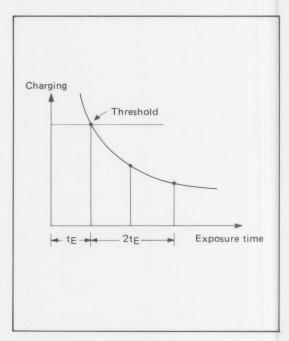
1.2 PROM programmer

Oki Electric employs a system whereby the various programmer available on the market are examined, and agreements reached with different programmer manufacturers. The purpose of this system is to check compatibility between programmer manufacturers and Oki Electric devices, and making modifications whenever required. Users are thus ensured trouble-free use.

In the event of EPROM trouble with Oki devices and approved programmer, problems will be handled by both Oki and driver manufacturer except where such problems have been caused purposely.

1.3 Erasure

Erasure of data written in the MSM2716AS can be effected by ultra-violet radiation of the memory element. In this case, the charge is discharged into the substrate or electrode by the ultra-violet energy, but note that the following erasure conditions must be met. If a memory which has not been properly erased is used, writing problems and operating failures are likely to arise. Also note that excessively long erasure times (of several hours duration) can also result in failure.



Lengthy exposure to direct sunlight can also result in loss of bits. Direct exposure of MSM2716 to the strong summer sun for a single day can result in bit changes. Although normal fluorescent lights have practically no effect, light rays beamed onto elements can cause special changes. It is therefore recommended that the glass face be covered with a screening label.

2. EPROM Handling

2.1 Defects caused by static electricity

The generation of static electricity on the EPROM glass face can result in changes in the memory contents. This, however, can be restored by brief exposure (several seconds) to ultra-violet radiation. But this exposure must be kept short. Exposure for 30 seconds or more can cause changes in the normal bits.

2.2 Handling precautions

- (1) Avoid carpets and clothes etc where static electricity is generated.
- (2) Make sure the programmer and mounting system are securely grounded.

- (3) Also make sure that any soldering iron employed is properly grounded.
- (4) Always carry in an electrically conductive plastic
- (5) Written ROMs are also to be kept in an electrically conductive plastic mat.
- (6) Do not touch the glass seal by hand since this can result in deterioration of the ultra-violet permeability required for erasure, and subsequently lead to poor erasure.

2.3 System debugging precautions

During system debugging, check operations with a voltage of $\pm 5\%$ (oscillating).

2 EPROM Handling

Vilaistuale situe bet beauer attached 1 F

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2.3 System debugging proceutions

During system debugging, check operations with a voltage of s8% (oscillating).

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

Magnetic tape single chip in o

(2) Use tage marks for file partitions when employ are used as standard (with multiple file formuts.

(3) Denote the completion of a magnetic tupe file by

2.3 Magnetic tage data format

(1) The data contained to a single file on majoret c taps must be inserted from the head address (0000)₁₀₄ or the device up to the final address in succession for a single chic.

(2) (a this case, the LSB of the data should correspond

(3) "I" birs in the data denote high device output while "0" describe low output

2.4: Mugootic tapo axamples

sgnatic tape and EPROM are used as standard (with SM2916 and MSM2932 employing only EPROM).

Magnetic tens specifications

1. Use the following types of inagnetic tape in magtic tape units compatible with IBM magnetic tape

Length: 2400 feet, 1200 feet or 600 fee

Indet that It

45 Channele 9 channels

4) Channels: 9 channels

can also be employed.

Block size: Integer multiples of 256 bytes as standard.

I block, I record is standard

Muti-lits formet (m chips)

\$\psi\$: tape mark

\$\psi\$: Tehsp date file 1

\$\psi\$: File 2

\$\psi\$: tape mark

\$\psi\$: The point file 1

\$\psi\$: File 2

\$\psi\$: File 3

\$\psi\$: File 2

\$\psi\$: File 2

\$\psi\$: File 3

\$\psi\$: File 4

\$\psi\$: File 5

\$\psi\$:

The mask ROM custom program code programming method is outlined below.

1. Usable media

- (1) Magnetic tape
- (2) EPROM

Magnetic tape and EPROM are used as standard (with MSM2916 and MSM2932 employing only EPROM).

2. Magnetic tape specifications

- 2.1 Use the following types of magnetic tape in magnetic tape units compatible with IBM magnetic tape units.
- (1) Length: 2400 feet, 1200 feet or 600 feet
- (2) No label
- (3) Width: 1/2 feet(4) Channels: 9 channels
- (5) Bit density: 800BPI standard, although 1600BPI
 - can also be employed.
- (6) Block size: Integer multiples of 256 bytes possible with 256 bytes as standard.
 - 1 block, 1 record is standard.

2.2 Magnetic tape format

- (1) The data for a single chip should not extend into several tapes. Data for several chips are allowed to be included in a single magnetic tape, multiple file format being permitted. In this case, include the data of a single chip in one file.
- (2) Use tape marks for file partitions when employing multiple file formats.
- (3) Denote the completion of a magnetic tape file by two successive tape marks.

2.3 Magnetic tape data format

- (1) The data contained in a single file on magnetic tape must be inserted from the head address (0000)_{hex} of the device up to the final address in succession for a single chip.
- (2) In this case, the LSB of the data should correspond to ${\rm D_0}$, and the MSB to ${\rm D_7}$.
- (3) "1" bits in the data denote high device output, while "0" denotes low output.

2.4 Magnetic tape examples

Multi-file format (m chips) * : tape mark 0 * * * * 0 1-chip data file 1 File m File 2 R R R R G G G G Block 2 Block 3 Block n-1 Block n

- 3. EPROM Specifications
- (1) MSM2716, MSM2764, Intel 2716, 2732, 2764 or equivalent device may be used.
- (2) Prepare 2 EPROMs containing identical data.

G

- EPROM Specifications
- (1) MSM2716, MSM2764, Intel 2716, 2732, 2764 or
 - beau ad years notween treated upon
 - ver brancos 2 EPROMs containing identical data

TERMINOLOGY AND SYMBOLS

		Dynamic RAM
		Vpo Vcc Ves
		A A.
		MIG
		TUD D
		aw-
		RAS
		CAS
		vas

TERMINOLOGY AND SYMBOLS

Pin Terminology

Term	EPROM	ROM	Static RAM	VDD, VCC	
Power supply voltage pin	V _{DD} , V _{CC} V _{GG} , V _{BB}	Vcc	Vcc		
Address input pin	A ₀ ~ A ₁₂	A ₀ ~ A ₁₃	A ₀ ~ A ₁₁	$A_0 \sim A_7$	
Data input pin			DI	DIN	
Data output pin	O ₀ ~ O ₇	D ₀ ~ D ₁₅	DO	D OUT	
Data input/output pin			1/O ₁ ~ 1/O ₈		
Chip enable pin	CE	CE	CE		
Output enable pin	OE	OE	OE		
Address enable pin		AE			
Chip select pin	cs		CS		
Write enable pin	WE		WE	WE	
Row address strobe pin				RAS	
Column address strobe pin				CAS	
Program input pin	Program, Vpp				
Data valid pin		DV			
Clock input pin		ФΤ			
Ground pin	V _{SS}	V _{SS}	V _{SS}	Vss	
Vacant terminal	NC	NC			

2. Absolute Maximum Ratings

	and the same of th			and the second second
MAR almany Term	EPROM	ROM	Static RAM	Dynamic RAM
Power supply voltage	V _{DD} , V _{CC} V _{GG} , V _{BB}	vcc	Vcc	V _{DD} , V _{CC}
asv asv	V _{SS}	V _{SS}	VSS	V _{SS}
Terminal voltage	V _T		VT	V _T
Input voltage	V _I MIV	VI HIV	VI	N VI W SAGAR THE
Output voltage	v _o	v _o av	V _O	Vo
Input current #33V				eta storaça voltag
Output current	JO.		10	sonatioaceo bec
Output shorting current	N	181		Ios
Load capacitance	тдоТ	Topr	510	perating temperat
Permissible loss	PD	PD	PD	PD
Operating temperature	Topr	Topr	Topr	Topr
Storage temperature	Tstg	Tstg	Tstg	Tstg

3. Recommended Operation Conditions

MAR amanya Term AR anata	EPROM	ROM	Static RAM	Dynamic RAM	
Power supply voltage	V _{DD} , V _{CC} V _{GG} , V _{BB}	Vcc	Vcc	V _{DD} , V _{CC}	
Vgg	V _{SS}	V _{SS}	V _{SS}	VSS	
"H" clock input voltage		TV		VIHC	
"H" input voltage	V _{IH} V	V _{IH}	VIH	VIH	
"L" input voltage	VIL OV	VIL OV	VIL	VIL	
Data storage voltage			Vccн	Input current	
Load capacitance		CL	CL	tnemus tubruO	
Fan-out 201	N	N	N	Output shorting car	
Operating temperature	Topr	Topr	Topr	Topr	
a9 a9	09	09		Pornissible toks	

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4. DC Characteristics

Term MAR almanyo MAR almaz	EPROM	ROM	Static RAM	Dynamic RAM
"H" output voltage	Voн	Voн	Voн	V _{OH}
"L" output voltage	VOL	VOL	VOL	VOL
"H" output current	tes	oat	ГОН	Chip select access to
"L" output current	BOA	801	emil	Chip enable access
Input leak current	ILI 00f	ILI SOT	ILI smit a	Output energiglace
Output leak current	ILO	ILO	ILO	I _{LO}
I/O leak current	ZHI	HO ₂	ILO	Output valed time
Program terminal current	I _{PP1} , I _{PP2}			mit out the combin
Peak power on current	HAT	I _{PO}	I _{PO} , I _{SBP}	Address froid time
207	IDD, ICC	Icc, Iccs	Icc, Icca	IDD1, ICC1, IBB1
Power supply current	I _{BB} , I _{CC1}	ICCA	CC1, CC2	IDD2, ICC2, IBB2
	filds		I _{SB}	IDD4, ICC4, IBB

5. AC Characteristics

(1) Read cycle

Term	EPROM	ROM	Static RAM	Dynamic RAM
Read cycle time	ноч	tc, tRC, tCYC	^t RC	tRC
Address access time	tACC	tAA, tACC	ta, tac, tacc, taa	author toution ".1"
Chip select access time	tco	tcs	tCO, tACS1, tACS2	Honus rogres "H"
Chip enable access time	tCE	tACE	^t AC	Transcoupe ".I'
Output enable access time	t _{OE}	t _{CO}	^t OE	oout leak cumant
Output setting time	1	tLZ	tCX, tLZ	nemup skel tugrut
Output valid time	tOH	tОН	tOH, tOHA	
Output disable time	^t DF	tHZ	tOTD, tHZ,	tOFF
Address set-up time		†AS	^t AS	
Address hold time	04	^t AH	^t AH	PLO NO 16WOO 344
Chip enable off time	lec. lees	pol-log!	tcc	
Chip enable pulse width	ADD	conl	tCE	aver supply curi
Power-up time		tpU	tpU	
Power-down time		tPD	tPD	
Address enable pulse width		†AE		
Data valid access time		tVA		
Data valid delay time		t _{VD}		
Clock delay time		tVH		
Clock pule width		tH		
Clock delay time		tL		
Output delay time		tDD		
Output access time		tDA		
Output hold time		tDH		
Address enable set-up time		†AES		

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(2) Write Cycle

Term	Term EPROM ROM		Static RAM	Dynamic RAM	
Write cycle time			twc	tWC	
Address set-up time	tAS		t _{AS} , t _{AW}		
Write pulse width	se width tpW twp		t _W , t _{WP}	t _{WP}	
Write recovery time			twR		
Data set-up time	t _{DS}		t _{DS} , t _{DW}	t _{DS}	
Data hold time	hold time tDH tDH		^t DH	^t DH	
tput off time t _{DF} t _{OTW} , t _{WZ}		tOFF			
Chip select set-up time	tcss		tcw		
Address hold time	^t AH		t _{AH} , t _{WR}		
Chip enable off time			tcc		
Chip enable pulse width			tCW, tCE		
Write enable set-up time			tws		
Write enable read time			tWCL		
Write enable hold time			tWH		
Address/write enable setting time			^t AW		
Write enable output activation			tow		
Output enable set-up time	tOES				
Output enable hold time	^t OEH				
Program read delay time	tDPR				
Output enable delay time	^t OE				
Chip enable data valid time	t _{DV}				
Program pulse rising edge time	tPRT				
Program pulse falling edge time	tPFT				
Vpp restoration time	tVR				
Chip enable hold time	^t CH				

(2) Write Cycle

DATA SHEET

DATA SHEET

MOS

RAMS



MSM3716 AS/RS

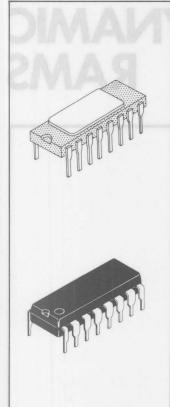
16384 WORD x 1 BIT DYNAMIC RAM (E3-S-001-32)

GENERAL DESCRIPTION

The Oki N-MOS integrated circuit MSM3716 AS/RS is an address multiplex type dynamic RAM with a 16,384 word x 1-bit configuration, featuring a wide operational margin and high-speed low power consumption while using a single transistor.

FEATURES

- 16,384 words x 1 bit
- 150ns access time and 375ns cycle time (MSM3716-2AS/RS)
 200ns access time and 375ns cycle time (MSM3716-3AS/RS)
- Standard 16-pin layout
- Low power consumption: 528mW (operation), 20mW (standby)
- Output data controlled by CAS only, while system design freedom is increased by not latch at cycle end.
- Read modify write, RAS only refresh and page mode operations possible.
- TTL compatible low capacitance for all inputs.
- 128 refresh cycle.



PIN CONFIGURATION (Top View) 1 16 2 15 14 3 4 13 5 12 6 11 7 10 8 9

1	V _{BB}	9	Vcc
2	D _{IN}	10	A ₅
3	WRITE	11	A ₄
4	RAS	12	A ₃
5	Ao	13	A ₆
6	A ₂	14	DOUT
7	A	25	CAS
8	V _{DD}	16	V _{SS}

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

 $(Ta = 25^{\circ}C)$

	Rating	.xsN	Symbol	Conditions	Symbol	Value	Unit
	Am	40	V _{DD}		roat	-1.0 ~ +15.0	
			Vcc	Respect to Vss	teet	-1.0 ~ +15.0	roq epine
Pauvas aupaliu valtas		200	V _{BB}	Respect to Vss V _{DD} - Vss	> 0 · 0	0 ~ -20.0	medo Buta
Power supply voltage	ge	V _{DD}		saai	- 0.5 ~ +20.0	V	
		10	Vcc	Pospost to Van	loca	− 0.5 ~ +20.0	agus 19vy
		001	Vss	DONT - High Impedance	engl	-0.5 ~ +20.0	em ydba
Input vo	oltage	27	VI		soo!	-0.5 ~ +20.0	
Output voltage		10	Vo	Respect to V _{BB}	erval	-0.5 ~ +20.0	rea distri
Storage	temperatu	e 000	Tstg		rnal	− 55 ~ +150	°C
Permissi	ble loss	29	PD		America I	1	W

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol Conditions		Recommended Operating Conditions			
		Min.	Тур.	Max.	alue H	
Power supply voltage	V _{DD}	700-01-01	10.8	12.0	13.2	
	Vcc	V _{CC} V _{BB} V _{IHC} Vss = 0	4.5	5.0	5.5	V
Busestas finomic returns delta sect 18	V _{BB}		-4.5	-5.0	-5.5	
"H" clock input voltage (note 1)	VIHC		2.7		6.0	
"H" input voltage (note 2)	VIH		2.4		6.0	
"L" input voltage (note 3)	VIL		-1.0		0.8	
Operating temperature	Topr		0		70	°C

Notes: 1. RAS, CAS and WRITE inputs

2. $A_0 \sim A_6$ and D_{IN} inputs 3. All inputs

DC CHARACTERISTICS

 $(V_{DD} = 12.0V \pm 10\%, V_{CC} = 5.0V \pm 10\%, V_{BB} = -5.0V \pm 10\%, V_{SS} = 0V, T_{a} = 0 - 70^{\circ}C)$

Parameter	Complete	Canditions	Special F	Ratings	Unit	Note
Farameter	Symbol	Conditions	Min.	Max.	Sating	
0.81+ - 0.1- I _D		Respect to Vis	ggV	40	mA	4
Average power supply current during operation	Icc1	t _{RC} = 375 ns	Vec			5
0.02	I _{BB1}	Respect to Vss Vgg - Vs	86V	200	μΑ	Private a
-0.5 ·· +20.0	I _{DD2}	500	aav	1.5	mA	
Power supply current during standby mode	I _{CC2}	RAS = VIHC	-10	10	μΑ	
	I _{BB2}	DOUT = High Impedance	asV.	100	μΑ	
-0.5 ~ +20.0	I _{DD3}	Respect to Veg	IV.	27	mA	4
Refresh power supply current	ICC3	t _{RC} = 375 ns	-10	10	μА	y sugaro-
	I _{BB3}		gseT	200	μΑ	Storage
	I _{DD4}	DAG - V	09	29	mA	4
Page mode power supply current	ICC4	RAS = V _{IL}				5
	I _{BB4}	tpC = 225 ns		200	μΑ	
Input leak current	I _{L1}	$V_{BB} = -5V$ 0 \le V ₁ < 6.0V	-10	10	μΑ	ECOM
Output leak current	ILO	$\begin{array}{c} D_{OUT} = Disable \\ 0 \le V_0 \le 5.5V \end{array}$	-10	10	μΑ	
"H" output voltage	VOH	I _O = -5 mA	2.4		V	
"L" output voltage	VOL	I _O = 4.2 mA		0.4	V	

Notes: 4. IDD1, IDD3 and IDD4 depend on cycle time.

 I_{CC1} and I_{CC4} are changed by output load. Vcc is connected to D_{OUT} at low impedance during reading of "H" level data.

<u>y</u>

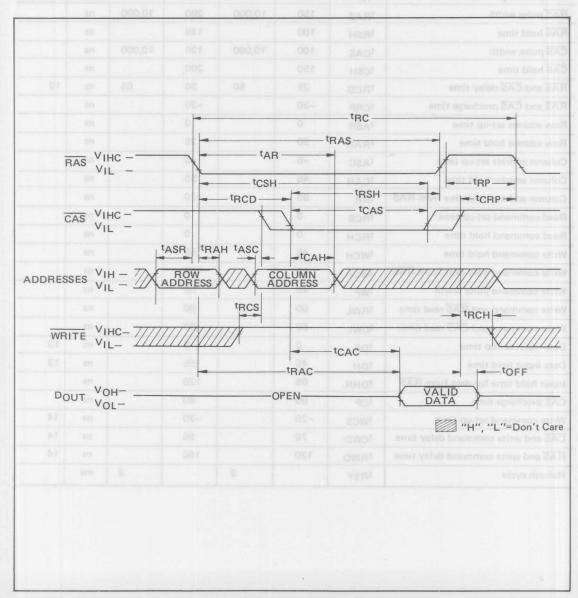
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

 $(V_{DD} = 12.0V \pm 10\%, V_{CC} = 5.0V \pm 10\%, V_{BB} = -5V \pm 10\%, V_{SS} = 0V, T_{a} = 0 \sim 70^{\circ}C)$ (Notes; 6, 7. 8)

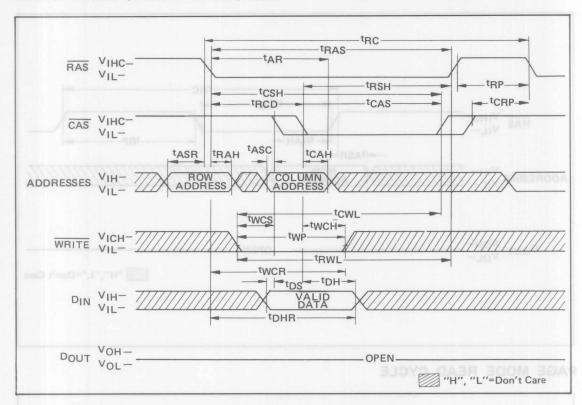
Parameter	Cumbal	MSM3716-2AS/RS		MSM371	6-3AS/RS	Units	Note
Parameter	Symbol	Min.	Max.	Min.	Max.	Offics	14016
Random read/write cycle time	tRC	375		375	30 AV = QL 1=001 + 11	ns	17.37
Read and write cycle time	tRWC	375	yd basme	375	MAX) is the	ns	gr
Page mode cycle time	tPC	170	- 57/5 min	225	CAC	nd Set n	200
Access time from RAS	tRAC	e cycle.	150	לערות ופסכ	200	THW	9, 11
Access time from CAS	tCAC	paiyliong	100	ou ais OM	135	ns	10, 11
Output turn-off delay time	tOFF	0	40	0	50	ns	
Rise and fall time	tŢ	3	35	3	50	ns	
RAS precharge time	tRP	100		120		ns	D GA
RAS pulse width	tRAS	150	10,000	200	10,000	ns	
RAS hold time	tRSH	100		135		ns	
CAS pulse width	tCAS	100	10,000	135	10,000	ns	
CAS hold time	tCSH	150		200		ns	
RAS and CAS delay time	tRCD	25	50	30	65	ns	12
RAS and CAS precharge time	tCRP	-20		-20		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	20		25		ns	
Column address set-up time	tASC	-5	AA.	-5	- 01	ns	
Column address hold time	tCAH	45	14801	55		ns	
Column address hold time from RAS	tAR	95	- cont-	120		ns	
Read command set-up time	tRCS	0	7	0		ns	
Read command hold time	tRCH	0	+	0		ns	
Write command hold time	tWCH	45	1 TASC	55		ns	
Write command hold time from RAS	twcR	95		120	100-1	ns	
Write command pulse width	tWP	45	F-/W/	55	4/14-	ns	
Write command and RAS read time	†RWL	60	SDRF	80		ns	
Write command and CAS read time	tCWL	60	17 100	80	TTTT _0	ns	
Data input set-up time	tDS	0	1	0	7077	ns	13
Data input hold time	†DH	45		55		ns	13
Input hold time for data from RAS	tDHR	95		120		ns	
CAS precharge time	tCP	60	9	80	- 71	ns	da
Write command set-up time	twcs	-20		-20		ns	14
CAS and write command delay time	tCWD	70		95		ns	14
RAS and write command delay time	tRWD	120		160		ns	14
Refresh cycle	tREF		2		2	ms	

- NOTES: 6. Normal memory operation may not be possible unless at least 8 cycles of operation are performed after the power is switched on.
 - 7. AC measurements when $t_T = 5ns$.
 - 8. Prescribed timing input levels of VIHC (MIN), VIH (MIN) and VIL (MAX).
 - 9. In the case of $t_{RCD} \le t_{RCD}$ (MAX); t_{RAC} is increased only for $t_{RCD} t_{RCD}$ (MAX) for $t_{RCD} > t_{RCD}$ (MAX) case.
 - 10. For tRCD ≥ tRCD (MAX) case.
 - 11. For 2TTL + 100pF load case.
 - 12. t_{RCD} (MAX) is the value guaranteed by t_{RAC} (MAX), and when t_{RCD} > t_{RCD} (MAX) it is distributed by t_{CAC}.
 - 13. t_{DS} and t_{DH} are specified by the CAS falling edge during the write cycle (early write), and by the WRITE falling edge during read modify write cycle.
 - 14. twcs, tcwp and tRwp are not parameters specifying operational limits. twcs ≥ twcs (MIN) results in write cycle (early write) with high impedance output. tcwp ≥ twcs (MIN) and tRwp ≥ tRwp (MIN) result in read modify write cycle.

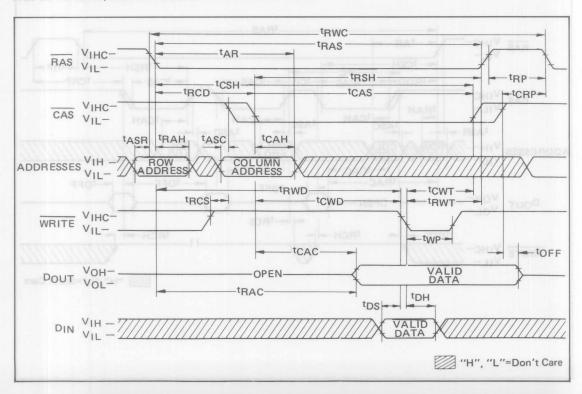
READ CYCLE



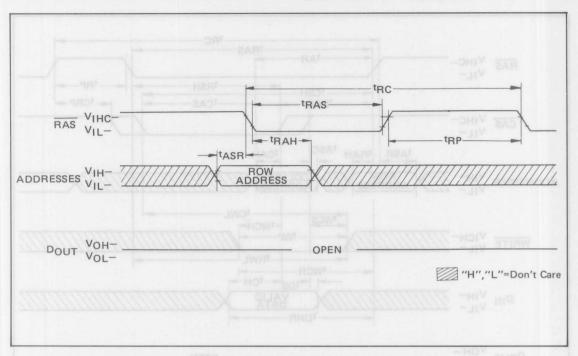
WRITE CYCLE (EARLY WRITE) OHIV = 2AO BLOYD HEBRABR "YJMO-BAR"



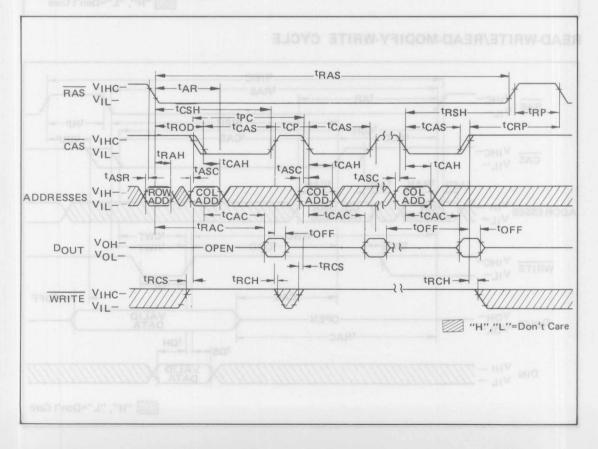
READ-WRITE/READ-MODIFY-WRITE CYCLE



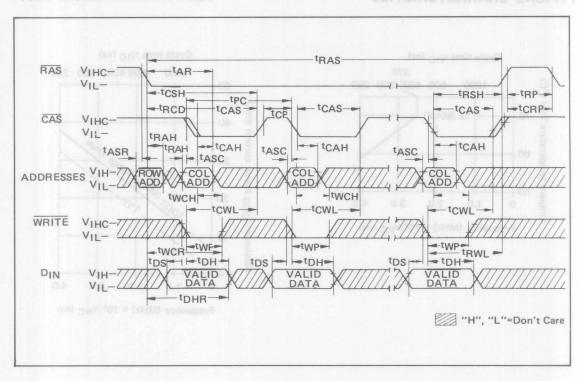
"RAS-ONLY" REFRESH CYCLE CAS = VIHC, WRITE = Don't Care



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

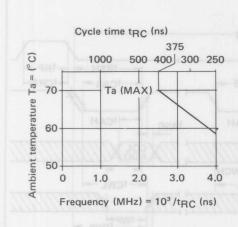


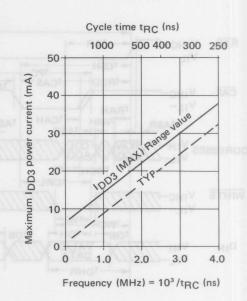
TERMINAL CAPACITANCE CHARACTERISTICS

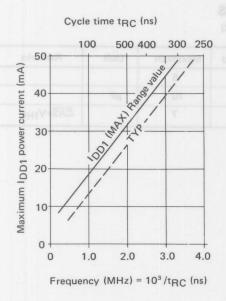
 $(V_{DD} = 12.0V \pm 10\%, V_{SS} = 0V, V_{BB} = 5.0V \pm 10\%, Ta = 0 \sim 70^{\circ}C)$

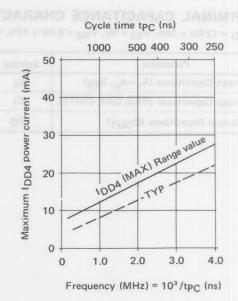
Parameter	Symbol	Standard	Maximum	Unit	Remarks
Input Capacitance (A ₀ ~A ₆ , D _{IN})	CI	4	5		
Input Capacitance (RAS, CAS, CRITE)	CI	8	10	pF	- DA 3
Output Capacitance (D _{OUT})	CO	5	7	1/4	CAS=VIHC

TYPICAL CHARACTERISTICS









MSM3732 AS/RS

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S-002-32)

GENERAL DESCRIPTION

The Oki MSM3732H/L is a fully decoded, dynamic NMOS random access memory organized as 32,768 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM3732 to be housed in a standard 16 pin DIP.

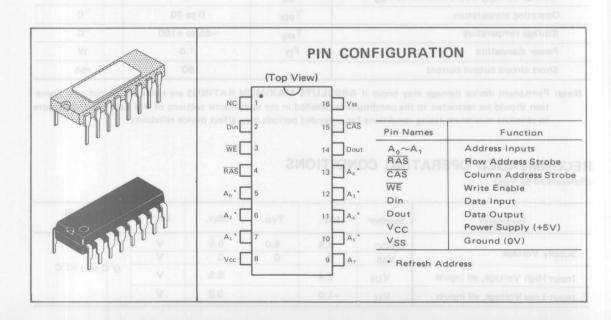
The MSM3732 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

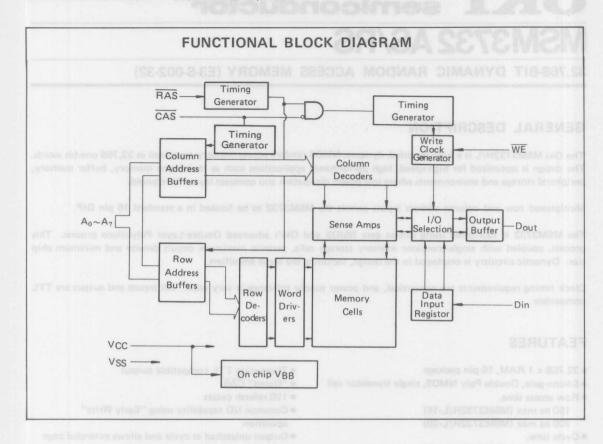
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 32,768 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time, 150 ns max (MSM3732H/L-15)
- 200 ns max (MSM3732H/L-20)
 Cycle time,
 270 ns min (MSM3732H/L-15)
 330 ns min (MSM3732H/L-20)
- Low power: 248 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load

- Three-state TTL compatible output
- "Gated" CAS
- 128 refersh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, RAS-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance





ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	VIN, VOUT	-1 to +7	V
Voltage on V _{CC} supply relative to V _{SS}	Vcc	-1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Power dissipation	PD	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Operating Temperature		
Supply Voltage	Vcc	4.5	5.0	5.5	V	TY THE		
	Vss	0	0	0	V			
Input High Voltage, all inputs	VIH	2.4		6.5	V	0°C to +70°C		
Input Low Voltage, all inputs	VIL	-1.0		0.8	V			

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current (RAS, CAS cycling; tRC = min.)	I _{CC1}	mbol Units	45	mA	die S
Standby Current Power supply current (RAS = CAS = VIH)	I _{CC2}	am qai	5.0	mA	Refresh period Rendom read or
Refresh Current Average power supply current (RAS cycling, CAS = V _{IH} ; t _{RC} = min.)	I _{CC3}	in pwis	35	mA	Read-write cycle Page mode cycle
Page Mode Current* Average power supply current (RAS = V _{IL} , CAS cycling; tp _C = min.)	I _{CC4}	IR DAI	42		Access time from Access time from Output buffer to
Input Leakage Current Input leakage current, any input $(0V \le V_{IN} \le 5.5V$, all other pins not under test = $0V$)	E ILI ₁	-10	10	μА	Transition time RAS precharge ti RAS pulse width
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le 5.5V$)	I _{L0}	-10 Hai	10	μА	RAS hold time CAS precharge ti
Output Levels Output high voltage (IOH = -5 mA) Output low voltage (IOL = 4.2 mA)	V _{OH} V _{OL}	2.4	0.4	V	CAS pulse wide CAS hold time

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

 $(T_a = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Тур.	Max.	Unit
Input Capacitance (A ₀ ~ A ₇ , D _{IN})	CIN1	4.5	5	pF
Input Capacitance (RAS, CAS, WE)	CIN2	7	10	pF
Output Capacitance (DOUT)	COUT	5	7	pF

Capacitance measured with Boonton Meter.

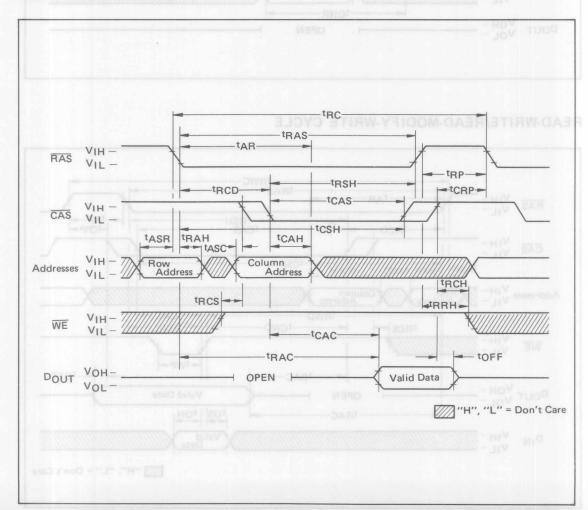
AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended
Operating conditions

Para Anti	Const	I le 'te	MSM3732-15		MSM3732-20		Net	
Parameter	Symbol	Units	Min.	Max.	Min.	Max.	Note	
Refresh period	tREF	ms	enal	2		2	mayius za vles	
Random read or write cycle time	tRC	ns	270		330	(44)	AS-	
Read-write cycle time	tRWC	ns	270		330		inathu	
Page mode cycle time	tPC	ns	170	Loiro	225	nus yiqqu	E ISHYO	
Access time from RAS	tRAC	ns		150		200	4,6	
Access time from CAS	tCAC	ns	1001	100	ant	135	5,6	
Output buffer turn-off delay	tOFF	ns	0	40	0	50	10/1	
Transition time	tT	ns	3	35	3	50	J ages	
RAS precharge time	tRP	ns	100	ton	120	no its ,Vi	azi	
RAS pulse width	tRAS	ns	150	10,000	200	10,000	VO=	
RAS hold time	tRSH	ns	100		135	Carrent	erges A lea	
CAS precharge time	tCP	ns	60		80	(V2)	N 10154	
CAS pulse width	tCAS	ns	100	10,000	135	10,000	afavi	
CAS hold time	tCSH	ns	150	(,0	200	HOI) egg	fov.rip	
RAS to CAS delay time	tRCD	ns	20	50	25	65	7	
CAS to RAS precharge time	tCRP	ns	0	negalbee	0	no Insbn	s depa	
Row Address set-up time	tASR	ns	0		0			
Row Address hold time	tRAH	ns	20		25	a	MA	
Column Address set-up time	tASC	ns	0		0	- jxHh	1 = 1	
Column Address hold time	tCAH	ns	45		55	Automa val		
Column Address hold time referenced to RAS	tAR	ns	95	Pilit	120	A) sones	caqsO	
Read command set-up time	tRCS	ns	0	1396	0	Arty sones	paqu.	
Read command hold time	tRCH	ns	0		0	De Bangrio	iquu.	
Write command set-up time	twcs	ns	-10	M netec	-10	measured	8	
Write command hold time	twcH	ns	45		55			
Write command hold time referenced to RAS	twcr	ns	95		120			
Write command pulse width	twp	ns	45		55			
Write command to RAS lead time	tRWL	ns	45		55			
Write command to CAS lead time	tCWL	ns	45		55			
Data-in set-up time	tDS	ns	0		0			
Data-in hold time	tDH	ns	45		55			
Data-in hold time referenced to RAS	tDHR	ns	95		120			
CAS to WE delay	tCWD	ns	60		80		8	
RAS to WE delay	tRWD	ns	110		145		8	
Read command hold time	tRRH	ns	20		25			

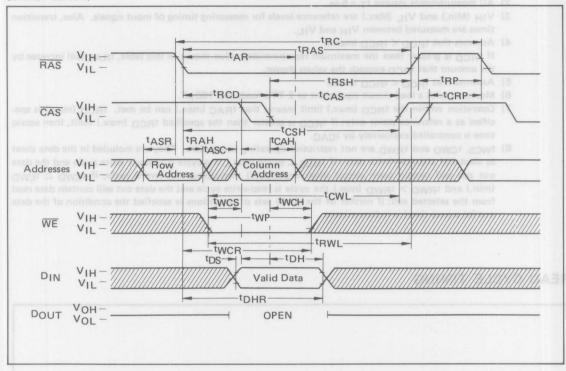
- NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Examples; RAS only) before proper device operation is achieved.
 - 2) AC measurements assume t_T = 5 ns.
 - 3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
 - 4) Assumes that t_{RCD} < t_{RCD} (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
 - 5) Assumes that tRCD < tRCD (max.)
 - 6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 - 7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
 - 8) twcs, tcwp and trwp are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if twcs ≥ twcs (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tcwp ≥ tcwp (min.) and trwp > trwp (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

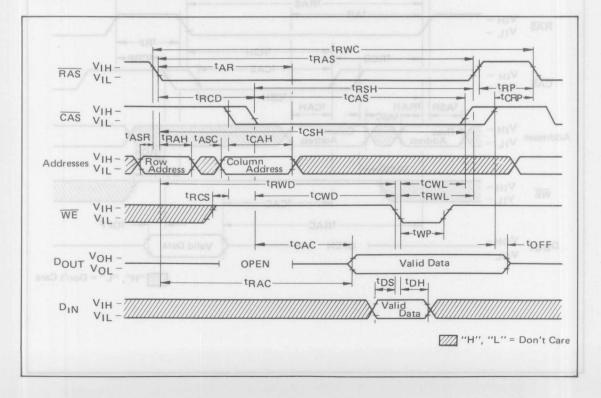


WRITE CYCLE TIMING

(EARLY WRITE)



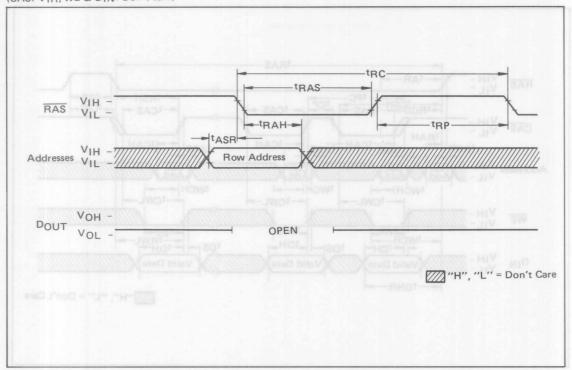
READ-WRITE/READ-MODIFY-WRITE CYCLE



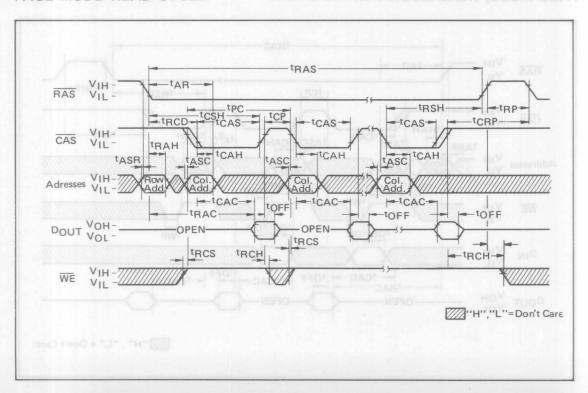
9

RAS ONLY REFRESH TIMING

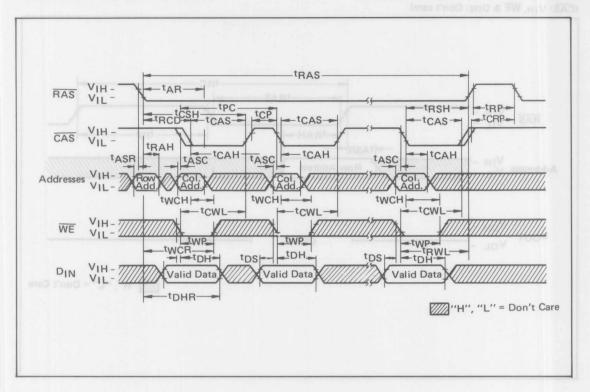
(CAS: VIH, WE & DIN: Don't care)



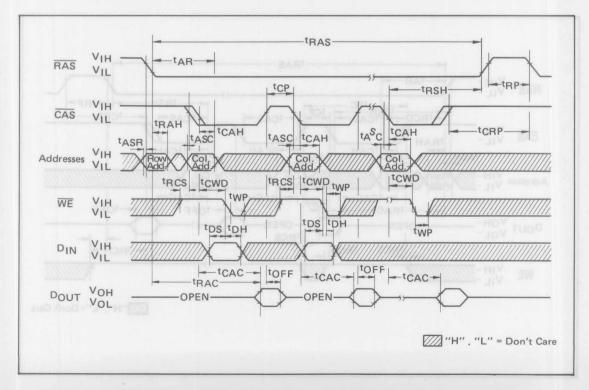
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

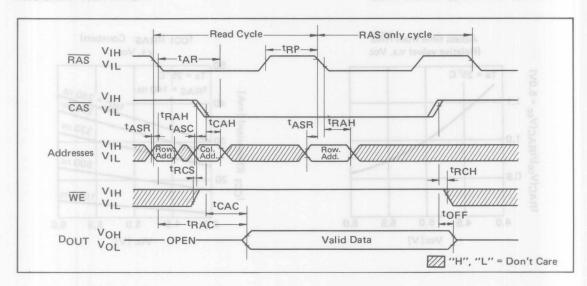


PAGE MODE, READ-MODIFY-WRITE CYCLE



9

HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of fifteen binary input address bits are required to decode any 1 of 32,768 storage cell locations within the MSM3732. Eight row-address bits are established on the input pins $(A_0\!\sim\!\!A_7)$ and latched with the Row Address Strobe (RAS). The seven column-address bits $(A_0$ through A_6) are established on the input pins and latched with the Column Address Strobe (CAS). All input addresses must be stable on or before the falling edge of RAS. CAS is internally inhibited (or "gated") by RAS to permit triggering of CAS as soon as the Row Address Hold Time (tRAH) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

One Column Address (A_7) has to be fixed at logic "0" (low level) for MSM3732L, and at logic "1" (high level) for MSM3732H.

Write Enable:

The read mode or write mode is selected with the \overline{WE} input. A logic high (1) on \overline{WE} dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3732 during a write or read-write cycle. The last falling edge of \overline{WE} or \overline{CAS} is a strobe for the Data In (DIN) register. In a write cycle, if \overline{WE} is brought low (write mode) before \overline{CAS} , DIN is strobed by \overline{CAS} , and the set-up and hold times are referenced to \overline{CAS} . In a read-write cycle, \overline{WE} will be delayed until \overline{CAS} has made its negative transistion. Thus DIN is strobed by \overline{WE} , and set-up and hold times are referenced to \overline{WE} .

Data Output:

The output buffer is three-state TTL compatible with

a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until \overline{CAS} is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of \overline{RAS} when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of \overline{CAS} when the transition occurs after t_{RCD} (max.). Data remain valid until \overline{CAS} is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3732 while maintaining RAS at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of RAS is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

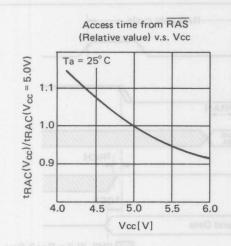
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7 . \overline{RAS} only refresh avoids any output during refresh because the output buffer is in the high impedance state unless \overline{CAS} is brought low. Strobing each of 128 row-addresses with \overline{RAS} will cause all bits in each rwo to be refreshed. Further \overline{RAS} -only refresh results in a substantial reduction in power dissipation.

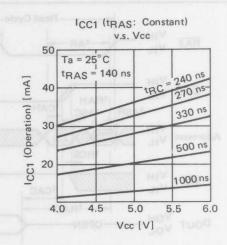
Hidden Refresh:

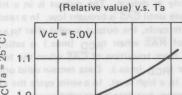
RAS ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{\text{CAS}}$ as V_{IL} from a previous memory read cycle.

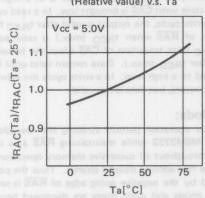
TYPICAL CHARACTERISTICS

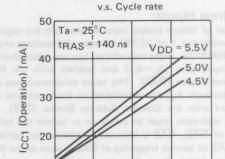






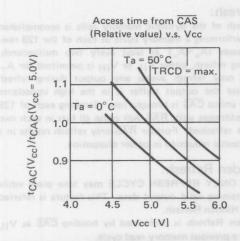
Access time from RAS

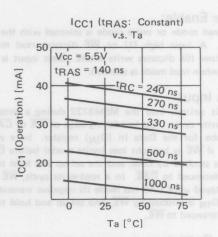




Cycle Rate (1/tRC) [MHz]

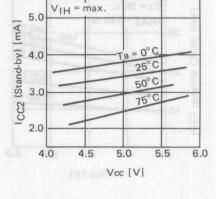
ICC1 (tRAS: Constant)

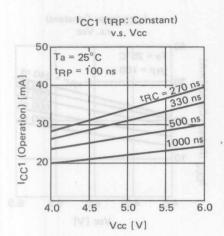


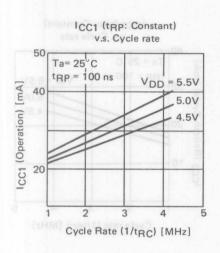


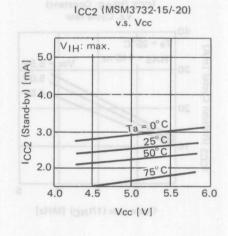
ICC2 (MSM3764-12)

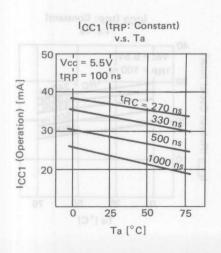
v.s. Vcc

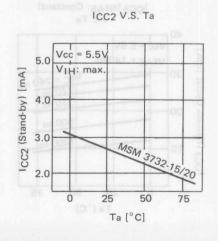


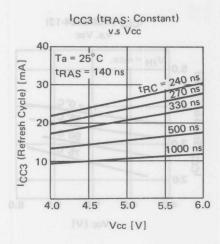


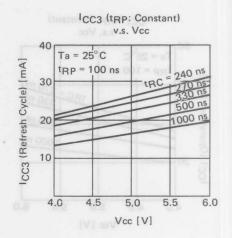


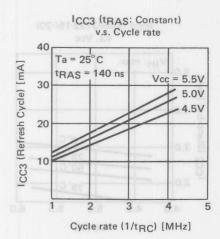


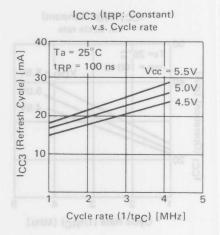




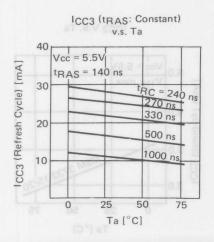


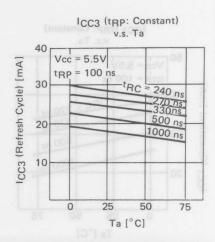




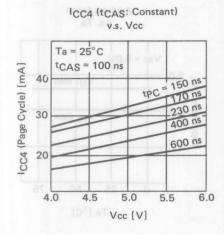


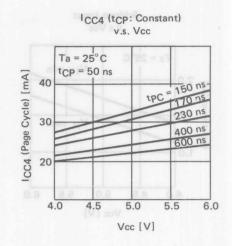


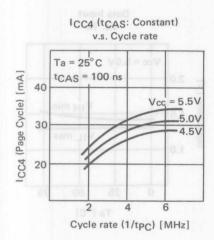


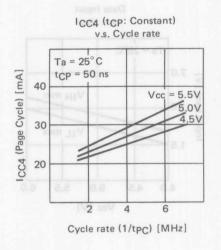


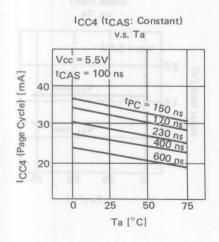


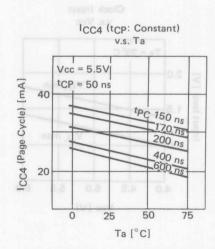


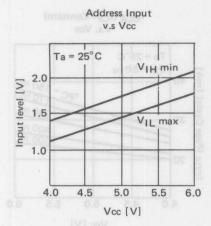


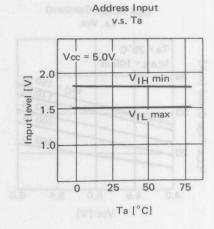


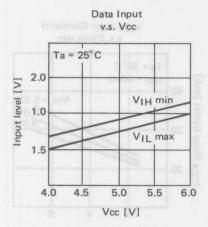


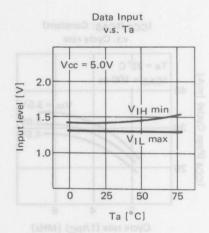


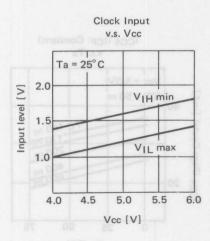


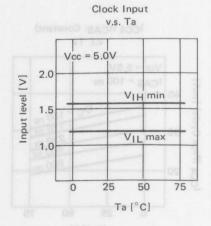


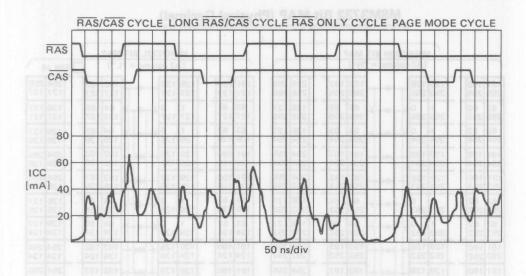












MSM3732 Bit MAP (Physical-Decimal)

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$(63 \leftarrow 0) \qquad (64 \rightarrow 127) \qquad (63 \leftarrow 0) \qquad (64 \rightarrow 127)$	91 31 63 30 91 30 91 30 91 29 63 29 63 28	132 190 131 62 131 62 130 190 129 62 129 62 128 190 128	132 129 131 1 131 1 130 129 130 129 129 1 128 128 129 128	132 128 131 0 131 0 130 128 130 128 129 0 129 0 128 128				132 192 131 64 131 64 130 192 130 192 129 64 128 192 128	132 193 131 65 130 193 130 193 129 65 128 193 128 (64 -	132 254 131 126 131 126 130 254 130 254 129 126 129 128 254 129	132 255 131 127 131 127 130 255 130 255 129 127 129 127 128 255 128	4 191 3 63 3 63 2 191 2 191 1 63 1 63 0	4 190 3 62 2 190 1 62 1 62 0 190 0 Refree (63	129 129 129 129 129 ((129 ((129) ((1	9 128 3 3 0 0 3 3 0 0 2 2 2 9 128 1 1 0 0 1 1 1 1 0 0 0 0 0 0 0 0		192 3 64 3 64 2 192 2 192 1 1 64 1 1 1 1 1 1 1 1	4 193 3 65 2 193 2 193 1 65 1 193 0	254 3 126 2 254 2 254 1 126 2 254 1 126 2 254 1 127 127	4 255 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
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$(63 \leftarrow 0) $	91 63 31 63 30 91 30 91 29 63 28 91 28	132 190 131 62 131 62 130 190 130 190 129 62 129 62 128 190 128	132 129 131 1 131 1 130 129 130 129 1 129 1 128 129 1 128	132 128 131 0 131 0 130 128 130 128 129 0 129 0 128 128				132 192 131 64 131 64 130 192 130 192 129 64 128 192 128	132 193 131 65 130 193 130 193 129 65 129 65 128 193 128 (64 -	132 254 131 126 130 254 130 254 129 126 128 254 129 126 128 27 127 127 130	132 255 131 127 130 255 130 255 129 127 128 255 128	4 191 3 63 3 3 63 2 191 2 191 1 63 0 191 0	4 190 3 62 3 62 2 190 1 62 1 62 0 PRefree (63	129 129 129 129 129 ((129 (120)	9 128 3 3 0 0 3 3 0 0 2 2 2 9 128 1 1 0 0 1 1 1 1 0 0 0 0 0 0 0 0		192 3 64 3 64 2 192 2 192 1 1 64 1 1 1 1 1 1 1 1	4 193 3 65 2 193 2 193 1 65 1 65 0 193 0	4 254 3 126 2 254 2 254 126 1 126 1 126 1 127 1 1 1 1 1 1 1 1 1 1 1 1 1	4 255 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
$(63 \leftarrow 0) \qquad (64 \rightarrow 127) \qquad (63 \leftarrow 0) \qquad (64 \rightarrow 127)$ $\begin{array}{cccccccccccccccccccccccccccccccccccc$	32 32 31 31 33 33 33 33 33 33 33 33 33 33 33	132 190 131 62 131 62 130 190 130 190 129 62 129 62 128 190 128	132 129 131 1 131 1 130 129 129 1 129 1 128 129 1 128 1 129 1 128	132 128 131 0 131 0 130 128 130 0 129 0 129 0 128 128			8	132 192 131 64 130 192 130 64 129 64 128	132 193 131 65 130 193 130 193 129 65 128 129 (64 (64 (Neg-in-	132 254 131 126 131 126 130 254 130 254 129 126 129 126 129 127 126 128	132 255 131 127 130 255 130 255 129 127 128 255 128	4 191 3 63 3 3 63 2 191 2 191 1 63 0 191 0	4 190 3 62 3 62 2 190 1 62 1 62 0 PRefree (63	129 129 129 129 129 ((129 (120)	9 128 3 3 0 0 3 3 0 0 2 2 2 9 128 1 1 0 0 1 1 1 1 0 0 0 0 0 0 0 0		192 3 64 3 64 2 192 2 192 1 1 64 1 1 1 1 1 1 1 1	4 193 3 65 2 193 2 193 1 65 1 65 0 193 0	4 254 3 126 2 254 2 254 126 1 126 1 126 1 127 1 1 1 1 1 1 1 1 1 1 1 1 1	4 255 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3

MSM3764 AS/RS

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S3-003-32)

GENERAL DESCRIPTION

The Oki MSM3764 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM3764 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MSM3764 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

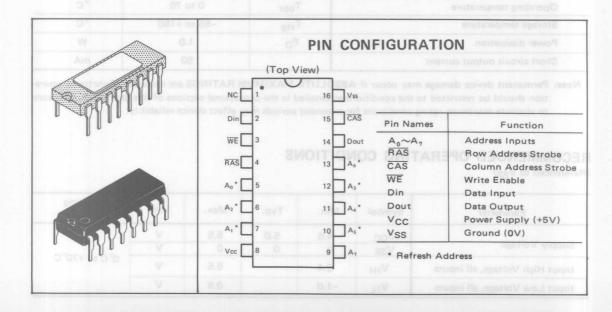
FEATURES

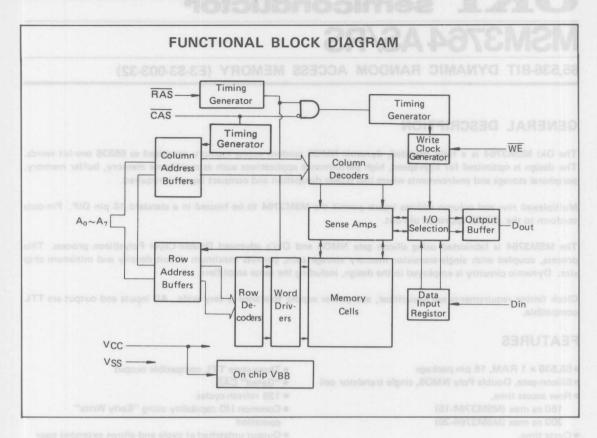
- 65,536 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- · Row access time,

150 ns max (MSM3764-15) 200 ns max (MSM3764-20)

- Cycle time,
 - 270 ns min (MSM3764-15) 330 ns min (MSM3764-20)
- Low power: 248 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load.

- Three-state TTL compatible output
- "Gated" CAS
- 128 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, RAS-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance





ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to VSS	VIN, VOUT	of evidence—1 to +7	All inpuVTTL or
Voltage on V _{CC} supply relative to V _{SS}	Vcc	-1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Power dissipation	PD	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Operating Temperature
(V0) brown0	Vcc	4.5	5.0	5.5	V	AVARIBER
Supply Voltage	VSS	0	0	0	V	
Input High Voltage, all inputs	VIH	2.4	1	6.5	V	0°C to +70°C
Input Low Voltage, all inputs	VIL	-1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current*					
Average power supply current (RAS, CAS cycling; t _{RC} = min.)	ICC1	arinU to	45	mA	Perein
Standby Current Power supply current	I _{CC2}	am	5.0	mA	boinsq riserted
(RAS = CAS = VIH)	270	EB	net len	a slava stru	Random read or h
Refresh Current Average power supply current	I _{CC3}	an s	35	mA	Read-write cycle!
(RAS cycling, CAS = VIH; tRC = min.)	170	30	pqt	emi	Page mode cycle t
Page Mode Current*		en :	DA FEE	RAS	Access time from
Average power supply current $(\overline{RAS} = V_{IL}, \overline{CAS} \text{ cycling}; tp_C = min.)$	ICC4	an (42	mA A	Access time from
Input Leakage Current	8	- arr	110		emit noitiener?
Input leakage current, any input $(0V \le V_{IN} \le 5.5V$, all other pins not	I _{LIO1}	-10	10	μΑ	RAS preclunge tin
under test = 0V)	150	100	an mr		distributed on ZAB
Output Leakage Current (Data out is disabled,	ILO	-10	10	μΑ	RAS held time
$0V \le V_{OUT} \le 5.5V$	08	-100	401	90	CAS precharge tile
Output Levels	100	an a	PCAS		CAS pulse width
Output high voltage (IOH = -5 mA)	Voн	2.4	HE 37	V	CAS hold time
Output low voltage (IOL = 4.2 mA)	VOL	200	0.4	V	ALCOHOL: STR

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

 $(T_a = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	НАСТур.	Max.	A Unit
Input Capacitance (A ₀ ~ A ₇ , D _{IN})	CIN1	4.5	emb bl51 aenbi	AnmpE
Input Capacitance (RAS, CAS, WE)	C _{IN2}	7	10	pF
Output Capacitance (DOUT)	COUT	5	7	pF

Capacitance measured with Boonton Meter.

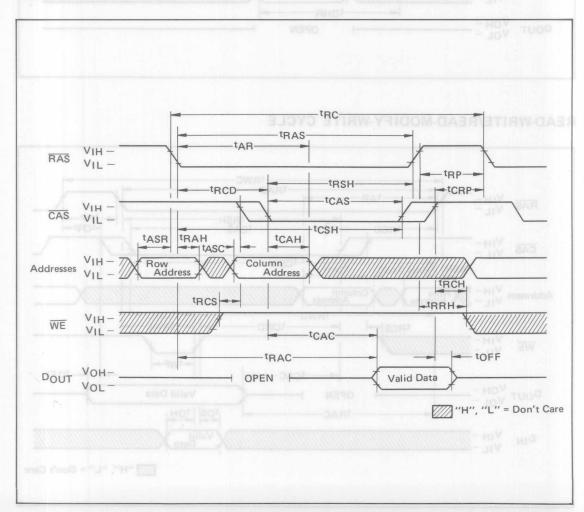
AC CHARACTERISTICS

With Motes 1, 2, 3 Under Recommended Operating conditions

	Operat							
Parameter	Symbol	Units	MSM	3764-15	MSM	3764-20	Note	
Parameter	Symbol	Units	Min.	Max.	Min.	Max.	Note	
Refresh period Am	tREF	ms	coo	2		2	tuo ylaque	
Random read or write cycle time	tRC	ns	270		330	18	V = EAD =	
Read-write cycle time	tRWC	ns	270		330		Current	
Page mode cycle time	tPC	ns	170	(min	225	apay curre S = Vant	ES mailan	
Access time from RAS	tRAC	ns		150	200	200	4,6	
Access time from CAS	tCAC	ns	100	100	- 10	135	5,6	
Output buffer turn-off delay	tOFF	ns	0	40	0	50	NO TIVE	
Transition time	tŢ	ns	3	35	3	50	BENEGO CU	
RAS precharge time	tRP	ns	100	20	120	ofto lis (V	VIN Z 8.8	
RAS pulse width	tRAS	ns	150	10,000	200	10,000	IV0 = 1001	
RAS hold time	tRSH	ns	100		135	inertu	Legislaga	
CAS precharge time	tCP	ns	60		80	(VE	EZTIN	
CAS pulse width	tCAS	ns	100	10,000	135	10,000	almon. L	
CAS hold time	tCSH	ns	150		200	HOI) ee	utlov dpid:	
RAS to CAS delay time	tRCD	ns	20	50	25	65	7	
CAS to RAS precharge time	tCRP	ns	0	bits gnibo	0	dent on p	C is depen	
Row Address set-up time	tASR	ns	0		0			
Row Address hold time	tRAH	ns	20		25	2	TANCE	
Column Address set-up time	tASC	ns	0		0	fsk	C, (= 1 M	
Column Address hold time	tCAH	ns	45		55	retarreter	9	
Column Address hold time referenced to RAS	tAR	ns	95	(1/1)	120	ncs (A ₀	ut Capacita	
Read command set-up time	tRCS	ns	0	1319	0	G 4 141 50 ni	toeden to	
Read command hold time	tRCH	ns	0		0	Mil abuen	Section Leads	
Write command set-up time	twcs	ns	-10	mild norm	-10	w benusser	8	
Write command hold time	tWCH	ns	45		55			
Write command hold time referenced to RAS	tWCR	ns	95		120			
Write command pulse width	tWP	ns	45		55			
Write command to RAS lead time	tRWL	ns	45		55			
Write command to CAS lead time	tCWL	ns	45		55			
Data-in set-up time	tDS	ns	0		0			
Data-in hold time	tDH	ns	45		55			
Data-in hold time referenced to RAS	^t DHR	ns	95		120			
CAS to WE delay	tCWD	ns	60		80		8	
RAS to WE delay	tRWD	ns	110		145		8	
Read command hold time referenced to RAS	tRRH	ns	20		25			

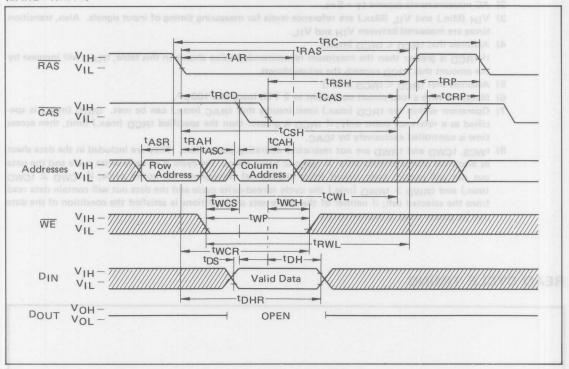
- NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Examples; RAS only) before proper device operation is achieved.
 - 2) AC measurements assume t_T = 5 ns.
 - 3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
 - 4) Assumes that tRCD < tRCD (max.).</p>
 If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the values shown.
 - 5) Assumes that t_{RCD} < t_{RCD} (max.)
 - 6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 - 7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
 - 8) twcs, tcwd and trwd are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if twcs ≥ twcs (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tcwd ≥ tcwd (min.) and trwd > trwd (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

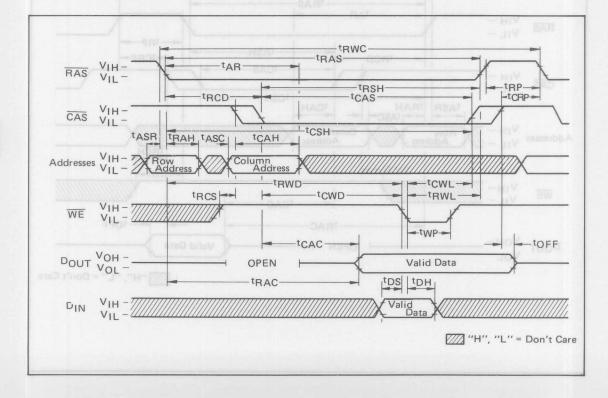


WRITE CYCLE TIMING

(EARLY WRITE)



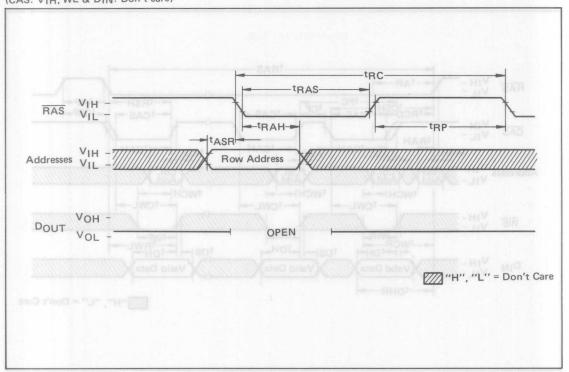
READ-WRITE/READ-MODIFY-WRITE CYCLE



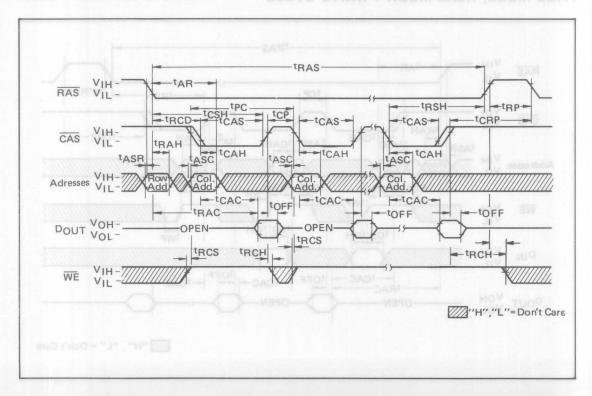
9

RAS ONLY REFRESH TIMING

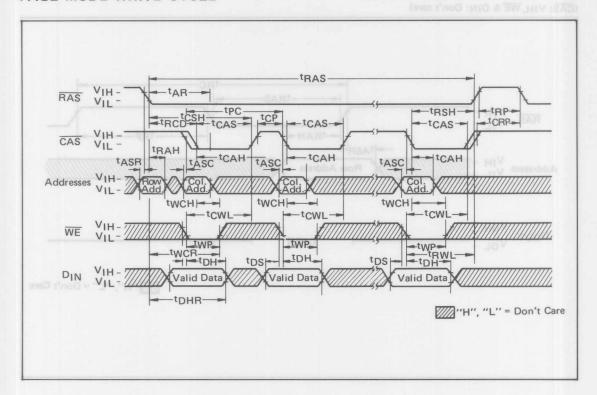
(CAS: VIH, WE & DIN: Don't care)



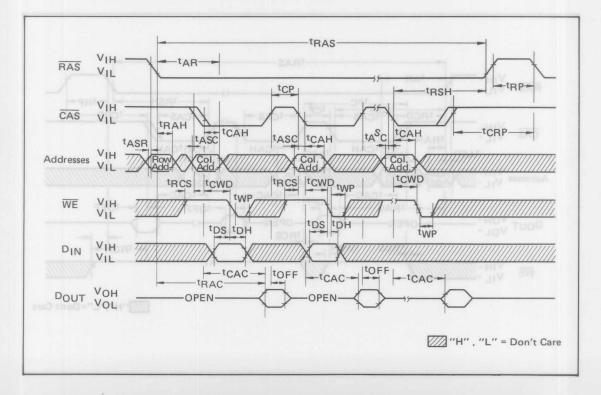
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

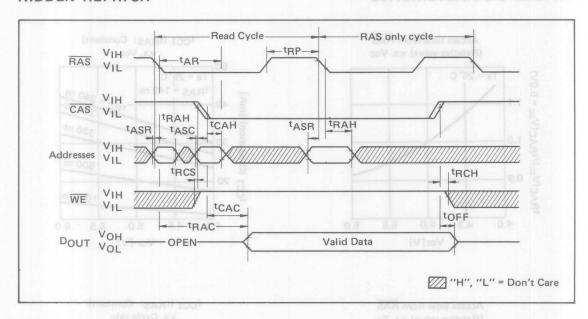


PAGE MODE, READ-MODIFY-WRITE CYCLE



9

HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764. Eight row-address bits are established on the input pins $(A_0{\sim}A_7)$ and latched with the Row Address Strobe (\overline{RAS}) . The eight column-address bits are established on the input pins and latched with the Column Address Strobe (\overline{CAS}) . All input addresses must be stable on or before the falling edge of \overline{RAS} . \overline{CAS} is internally inhibited (or "gated") by \overline{RAS} to permit triggering of \overline{CAS} as soon as the Row Address Hold Time (t_RAH) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the \overline{WE} input. A logic high (1) on \overline{WE} dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764 during a write or read-write cycle. The last falling edge of \overline{WE} or \overline{CAS} is a strobe for the Data In (D_{IN}) register. In a write cycle, if \overline{WE} is brought low (write mode) before \overline{CAS} , D_{IN} is strobed by \overline{CAS} , and the set-up and hold times are referenced to \overline{CAS} . In a read-write cycle, \overline{WE} will be delayed until \overline{CAS} has made its negative transistion. Thus D_{IN} is strobed by \overline{WE} , and set-up and hold times are referenced to \overline{WE} .

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the

same polarity as data-in. The output is in a high impedance state until \overline{CAS} is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of \overline{RAS} when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of \overline{CAS} when the transition occurs after t_{RCD} (max.). Data remain valid until \overline{CAS} is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764 while maintaining \overline{RAS} at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of \overline{RAS} is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

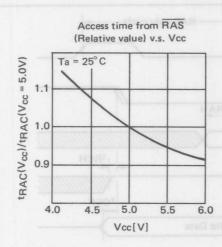
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses $(\mathsf{A_0}{\sim}\mathsf{A_6})$ at least every two milliseconds. During refresh, either $\mathsf{V_{IL}}$ or $\mathsf{V_{IH}}$ is permitted for $\mathsf{A_7}$. RAS only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{\mathsf{CAS}}$ is brought low. Strobing each of 128 row-addresses with RAS will cause all bits in each rwo to be refreshed. Further RAS-only refresh results in a substantial reduction in power dissipation.

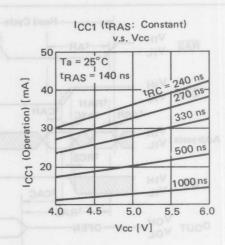
Hidden Refresh:

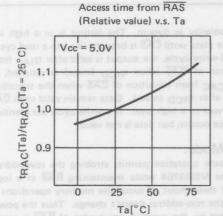
RAS ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

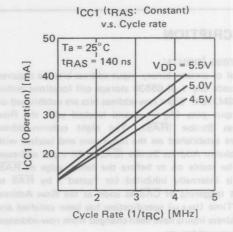
Hidden Refresh is performed by holding $\overline{\text{CAS}}$ as V_{IL} from a previous memory read cycle.

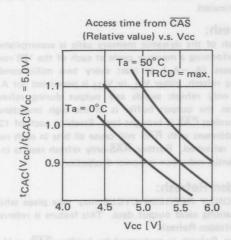
TYPICAL CHARACTERISTICS

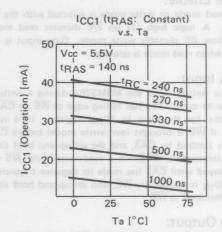


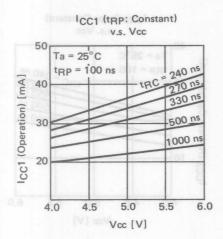


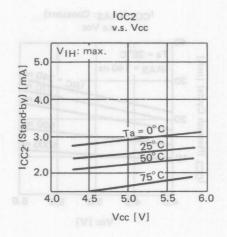


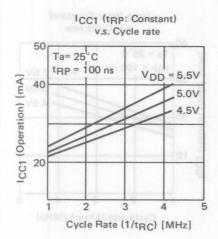


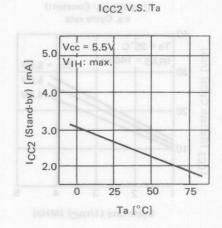


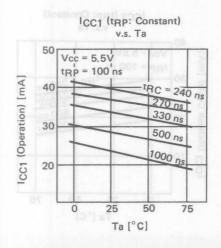


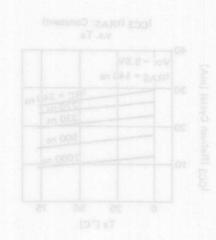


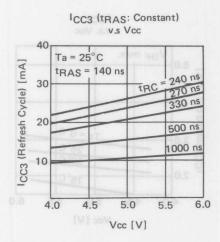


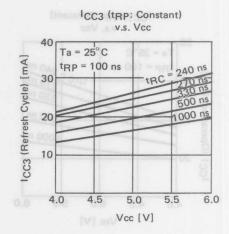


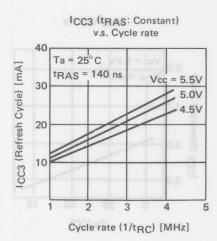


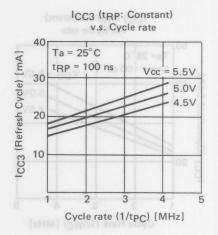


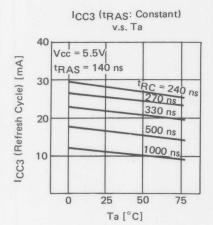


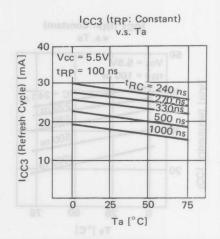




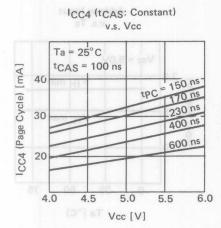


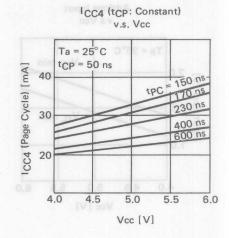


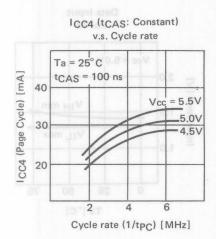


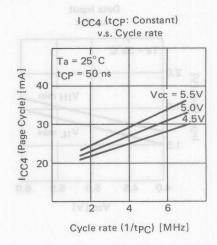


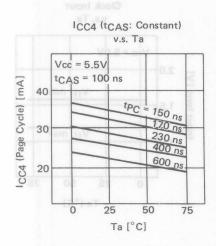


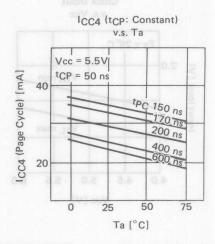




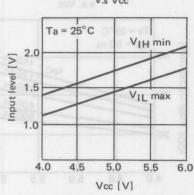




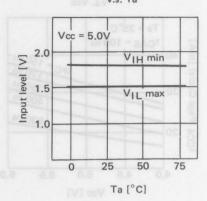




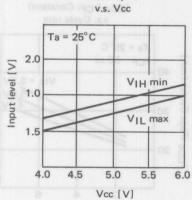
Address Input v.s Vcc



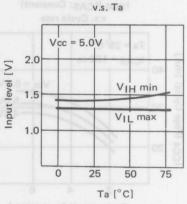
Address Input v.s. Ta

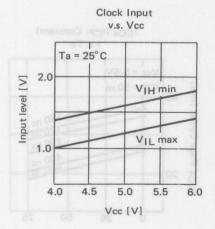


Data Input

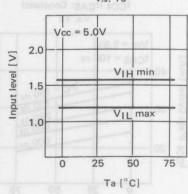


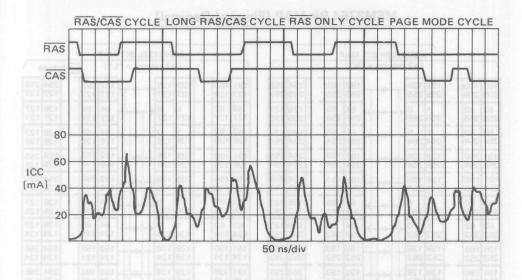
Data Input





Clock Input v.s. Ta





MSM3764 Bit MAP (Physical-Decimal)

_			IT MAP			MSM3732L I		RAS
	-	olumn =		Jan-V		[A7 column		PIN 16
91 190 55 255	129 128 255 255	•	192 193 255 255	254 255 255 255	191 190 127 127	129 128 127 127	192 193 127 127	254 255 127 127
63 62 55 255	1 0 255 255	101	64 65 255 255	126 127 255 255	63 62 127 127	1 0 0	64 65 127 127	126 127 127 127
63 62 54 254	1 0 254 254	0	64 65 254 254	126 127 254 254	63 62 126 126	1 0 126 126	64 65 126 126	126 127 126 126
91 190 54 254	129 128 254 254	704	192 193 254 254	254 255 254 254	191 190 126 126	129 128 126 126	192 193 126 126	254 255 126 126
91 190 53 253	129 128 253 253	704	192 193 253 253	254 255 253 253	191 190 125 125	129 128 125 125	192 193 125 125	254 255 125 125
63 62 53 253	1 0 253 253	0	64 65 253 253	126 127 253 253	63 62 125 125	1 0 125 125	64 65 125 125	126 127 125 125
63 62 52 252	1 0 252 252	0	64 65 252 252	126 127 252 252	63 62 124 124	1 0 0	64 65 124 124	126 127 124 124
91 190 52 252	129 128 252 252	70	192 193 252 252	254 255 252 252	191 190 124 124	129 128 124 124	192 193 124 124	254 255 124 124
91 190 51 251	129 128 251 251	70	192 193 251 251	254 255 251 251	191 190 123 123	129 128 123 123	192 193 123 123	254 255 123 123
91 190 32 132	129 128 132 132	704	192 193 132 132	254 255 132 132	191 190 4 4	129 128	192 193 4 4	254 255 4 4
	+		192 193	254 255	191 190	129 128	192 193	254 255 3 3
91 190 31 131	129 128 131 131	705	131 131	[131 [131]		3 3 3		
31 131 63 62	131 131		131 131 64 65 131 131	126 127 131 131	63 62 3 3	3 3 1 0 3 3	64 65	126 127
31 131 63 62 31 131 63 62	131 131 1 0 131 131 1 0		64 65 131 131 64 65	126 127 131 131 126 127	63 62	1 0 3 3	64 65 3 3 64 65	126 127
31 131 63 62 31 131	131 131 1 0 131 131	0	64 65 131 131	126 127 131 131	63 62 3 3	1 0 3 3	64 65 3 3	126 127 2 3 126 127
31 131 63 62 31 131 63 62 30 130 91 190	131 131 1 0 131 131 1 0 130 130 129 128	0	64 65 131 131 64 65 130 130 192 193	126 127 131 131 126 127 130 130 254 255	63 62 3 3 63 62 2 2	1 0 3 3 1 0 2 2	64 65 3 3 64 65 2 2 192 193	126 127 2 3 126 127 2 2 254 255
31 131 63 62 31 131 63 62 30 130 91 190 30 130 91 190	131 131 1 0 131 131 1 0 130 130 129 128 130 130 129 128	0	64 65 131 131 64 65 130 130 192 193 130 130 192 193	126 127 131 131 126 127 130 130 254 255 130 130 254 255	63 62 3 3 63 62 2 2 191 190 2 2	1 0 3 3 1 0 2 2 129 128 2 2 129 128	64 65 2 2 192 193 2 2 192 193	126 127 2 3 126 127 2 2 254 255 2 2 254 255
31 131 63 62 31 131 63 62 30 130 91 190 91 190 99 129 63 62	131 131 1 0 131 131 1 0 130 130 129 128 130 130 129 128 129 129 1 0	1 0	64 65 131 131 64 65 130 130 192 193 130 130 192 193 129 129 64 65	126 127 131 131 126 127 130 130 254 255 130 130 254 255 129 129 126 127	63 62 3 3 63 62 2 2 191 190 2 2 191 190 1 1 63 62	1 0 3 3 1 0 2 2 129 128 2 2 129 128 1 1	64 65 3 3 64 65 2 2 192 193 2 2 192 193 1 1 64 65	126 127 2 3 126 127 2 2 254 255 2 2 254 255 1 1 126 127
31 131	131 131 1 0 131 131 1 0 130 130 129 128 130 130 129 128 129 129 1 0 129 129	1 0	64 65 131 131 64 65 130 130 192 193 130 130 192 193 129 129 64 65 129 129 64 65	126 127 131 131 126 127 130 130 254 255 130 130 254 255 129 129 126 127 129 129 126 127	63 62 3 3 63 62 2 2 191 190 2 2 191 190 1 1 63 62 1 1	1 0 3 3 3 1 0 2 2 2 129 128 2 2 2 129 128 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	64 65 2 2 192 193 2 2 192 193 1 1 64 65 1 1 64 65 0 0	126 127 2 3 126 127 2 2 254 255 2 2 254 255 1 1 126 127 1 1 126 127
31 131 63 62 31 131 63 62 30 130 91 190 91 190 29 129 129 129 63 62 29 129 63 62 29 129 63 62 80 130	131 131 1 0 131 131 1 0 130 130 129 128 130 130 129 129 1 0 129 129 1 0 129 129 1 0 129 129 1 29 129		64 65 131 131 64 65 130 130 192 193 130 130 192 193 129 129 64 65 128 128 192 193	126 127 131 131 126 127 130 130 254 255 130 130 254 255 129 129 126 127 129 129 126 127 128 128 254 255	63 62 3 3 63 62 2 2 191 190 2 2 191 190 1 1 63 62 1 1 63 62 0 0	1 0 3 3 3 1 0 2 2 129 128 2 2 129 128 1 1 1 0 0 0 129 128	64 65 2 2 192 193 2 2 192 193 1 1 1 64 65 1 1 1 64 65 0 0	126 127 2 3 126 127 2 2 254 255 2 2 254 255 1 1 126 127 1 1 126 127 0 0 254 255
31 131 63 62 31 131 63 62 30 130 91 190 30 130 91 190 29 129 63 62 29 129 63 62 28 128 91 190 28 128	131 131 1 0 131 131 1 0 130 130 129 128 130 130 129 128 129 129 1 0 128 128 129 128 129 128 129 128 129 128 129 128 129 128 129 128		64 65 131 131 64 65 130 130 192 193 130 130 192 193 129 129 64 65 129 129 64 65 128 128 192 193 128 128	126 127 131 131 126 127 130 130 254 255 130 130 254 255 129 129 126 127 129 129 126 127 128 128 254 255 128 128	63 62 3 3 63 62 2 2 191 190 2 2 191 190 1 1 1 63 62 1 1 63 62 0 0 191 190 0 0	1 0 3 3 3 1 0 2 2 2 129 128 2 2 129 128 1 1 1 1 0 0 0 1 129 128 0 0 0	64 65 3 3 64 65 2 2 192 193 2 2 1 1 1 64 65 1 1 64 65 0 0 192 193 0 0	126 127 2 3 126 127 2 2 254 255 2 2 254 255 1 1 126 127 0 0 254 255 0 0
31 131 63 62 31 131 62 30 130 91 190 30 130 91 190 29 129 63 62 29 129 63 62 28 128 91 190 28 128 91 190 28 128	131 131 1 0 131 131 1 1 0 130 130 130 13		64 65 131 131 64 65 130 130 192 193 130 130 192 193 129 129 64 65 129 129 64 65 128 128 192 193 128 128	126 127 131 131 126 127 130 130 254 255 130 130 254 255 129 129 126 127 129 129 126 127 128 128 254 255 128 128	63 62 3 3 63 62 2 2 2 191 190 2 2 191 190 1 1 1 63 62 1 1 63 62 0 0	1 0 3 3 3 1 0 2 2 129 128 2 2 2 129 128 1 1 1 1 0 0 1 1 1 1 0 0 0 129 128 0 0	64 65 3 3 64 65 2 2 192 193 2 2 192 193 1 1 64 65 1 1 64 65 0 0 0 0	126 127 2 3 126 127 2 2 254 255 2 2 2 254 255 1 1 126 127 1 1 126 127 0 0 254 255 0 0
31 131 63 62 31 131 62 30 130 91 190 30 130 91 190 29 129 63 62 29 129 63 62 28 128 91 190 28 128 91 190 28 128	131 131 1 0 131 131 1 0 130 130 130 130		64 65 131 131 64 65 130 130 192 193 130 130 192 193 129 129 64 65 129 129 64 65 128 128 192 193 128 128	126 127 131 131 126 127 130 130 254 255 130 130 254 255 129 129 126 127 129 129 126 127 128 128 254 255 128 128	63 62 3 3 63 62 2 2 2 191 190 1 1 1 63 62 1 1 63 62 0 0 191 190 0 0	1 0 3 3 3 1 1 0 2 2 2 129 128 2 2 129 128 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	64 65 2 2 192 193 1 1 64 65 1 1 64 65 0 0 192 193 0 0 Refresh	126 127 2 3 126 127 2 2 254 255 2 2 254 255 1 1 126 127 0 0 254 255 0 0
31 131 63 62 31 131 62 30 130 91 190 30 130 91 190 29 129 63 62 29 129 63 62 28 128 91 190 28 128 91 190 28 128	131 131 1 0 131 131 1 1 0 130 130 130 13		64 65 131 131 64 65 130 130 192 193 130 130 192 193 129 129 64 65 129 129 64 65 128 128 192 193 128 128	126 127 131 131 126 127 130 130 254 255 130 130 254 255 129 129 126 127 129 129 126 127 128 128 254 255 128 128	63 62 3 3 63 62 2 2 2 191 190 1 1 1 63 62 1 1 63 62 0 0 191 190 0 0	1 0 3 3 3 1 1 0 2 2 2 129 128 2 2 129 128 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	64 65 2 2 192 193 1 1 64 65 1 1 64 65 0 0 192 193 0 0 Refresh	126 127 2 3 126 127 2 2 254 255 2 2 2 254 255 1 1 126 127 1 1 126 127 0 0 254 255 0 0
31 131 33 62 30 130 30 30 30 30 30 30	131 131 1 0 131 131 1 0 131 131 1 1 0 130 13	D, i Pin 8	64 65 131 131 64 65 130 130 192 193 130 130 192 193 129 129 64 65 129 129 64 65 128 128 192 193 128 128	126 127 131 131 126 127 130 130 254 255 130 130 254 255 129 129 126 127 129 129 126 127 128 128 254 255 128 128 128 128	63 62 3 3 63 62 2 2 2 191 190 1 1 1 63 62 1 1 63 62 0 0 191 190 0 0	1 0 3 3 3 1 1 0 2 2 2 129 128 2 2 129 128 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	64 65 2 2 192 193 1 1 64 65 1 1 64 65 0 0 192 193 0 0 Refresh	126 127 2 3 126 127 2 2 254 255 2 2 2 254 255 1 1 126 127 0 0 254 255 0 0

IMA.

MSM3764 AAS/ARS

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S-004-32)

GENERAL DESCRIPTION

The Oki MSM3764A is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM3764A to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

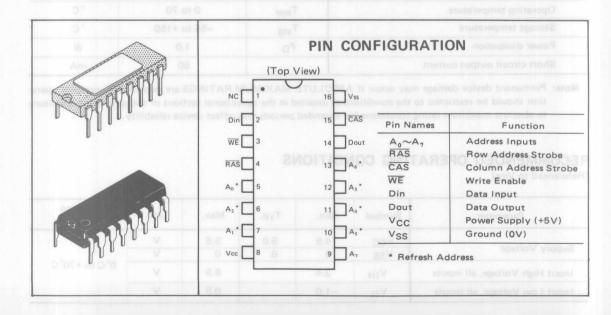
The MSM3764A is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

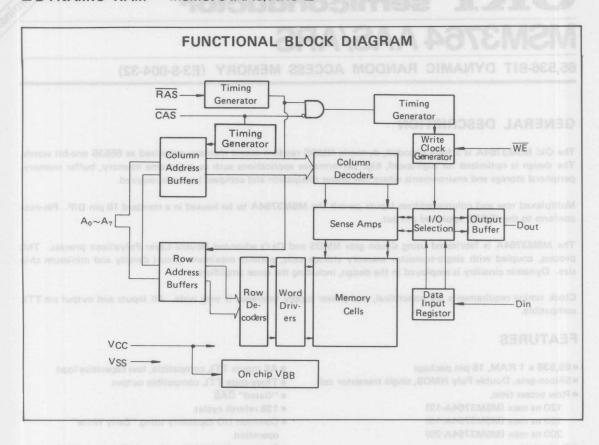
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 65,536 x 1 RAM, 16 pin package
- · Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
 - 120 ns max (MSM3764A-12)
 - 150 ns max (MSM3764A-15)
 - 200 ns max (MSM3764A-20)
- Cycle time.
 - 230 ns min (MSM3764A-12)
 - 260 ns min (MSM3764A-15)
 - 330 ns min (MSM3764A-20)
- Low power: 330 mW active,
 28 mW max standby
- Single +5V Supply, ±10% tolerance

- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 128 refersh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, RAS-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance





ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to VSS	V _{IN} , V _{OUT}	-1 to +7	V
Voltage on V _{CC} supply relative to V _{SS}	Vcc	-1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Power dissipation	PD	1.0	W
Short circuit output current	Lauret auctri	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Operating Temperature
Ground (DV)	Vcc	4.5	5.0	5.5	V	MAIN
Supply Voltage	VSS	0	0	0	V	
Input High Voltage, all inputs	VIH	2.4		6.5	V	0°C to +70°C
Input Low Voltage, all inputs	VIL	-1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current	I _{CC1}	Units Mis-	60	mA	rstemeter
(RAS, CAS cycling; tRC = min.)	2 1	am	3397		Refresh period
Standby Current		ns 230	180	emil els	Random reed or write cyc
Power supply current $(\overline{RAS} = \overline{CAS} = V_{IH})$	ICC2	ns 285	5.0	mA	sorit slove streeter
Refresh Current		ns [13])	341		age mode cycle time
Average power supply current (RAS cycling, CAS = VIH; tRC = min.)	1CC3	an .	40	mA	Access time from RAS
	00	201	DAG!		2A5 most switteens
Page Mode Current*	35	0 20	60	mA	the met withed tugruC
Average power supply current $(\overline{RAS} = V_{IL}, \overline{CAS} \text{ cycling}; tp_C = min.)$	ICC4	£ an	60	mA	Fransition time
Input Leakage Current		001 an	9.691		AS prechange time
Input leakage current, any input $(0V \le V_{IN} \le 5.5V$, all other pins not	officer	-10	10	μΑ	AAS pulse width
under test = 0V)		16 an	HSBI		RAS hold time
Output Leakage Current		da an	931	(alova)	CAS precharge time (Page
(Data out is disabled,	ILO	-10	10	μΑ	CAS pulse width
Output Levels		100 30	HED		OAS held sins
Output high voltage (IOH = -5 mA)	Voн	2.4	GO FF	V	TAS to CAS delay time
Output low voltage (IOL = 4.2 mA)	VOL	0 30	0.4	V	CAS to RAS procharge to

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

 $(T_a = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Тур.	Max.	Unit
Input Capacitance (A ₀ ~ A ₇ , D _{IN})	CIN1	4.5	5	pF
Input Capacitance (RAS, CAS, WE)	CIN2	7	10	pF
Output Capacitance (DOUT)	COUT	5	7	pF

Capacitance measured with Boonton Meter.

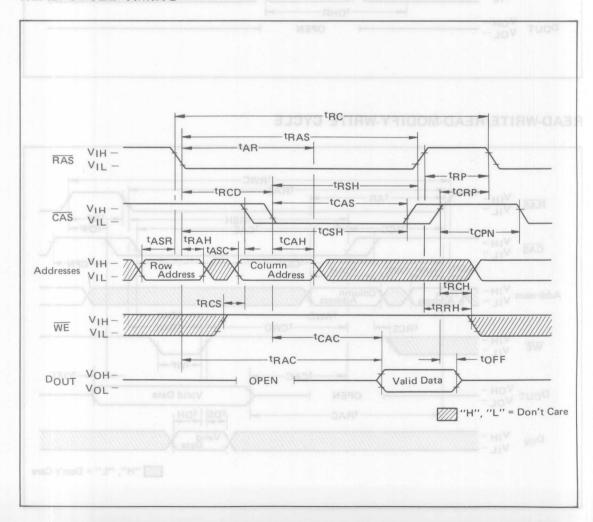
AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Powers - to -	Symbol	Unito	MSM3	764A-12	MSM3	764A-15	MSM3	3764A-20	NI-
Parameter	Symbol	Units	Min.	Max.	Min.	Max.	Min.	Max.	Note
Refresh period	tREF	ms		2		2	O.E. 181.C	2	AAS,
Random read or write cycle time	tRC	ns	230		260		330	V Current	dbmm
Read-write cycle time	tRWC	ns	255	1002	280		345	upply cut	19140
Page mode cycle time	tPC	ns	130		145		190	technology (%)	
Access time from RAS	tRAC	ns		120		150	in ylaq	200	4,6
Access time from CAS	tCAC	ns		60	(.nim	75	N = S	100	5,6
Output buffer turn-off delay	tOFF	ns	0	35	0	40	0	50	AL RES
Transition time	tT	ns	3	35	3	35	3	50	ZXP
RAS precharge time	tRP	ns	100		100		120	ud spakes	Jugn
RAS pulse width	tRAS	ns	120	10,000	150	10,000	200	10,000	Lindu
RAS hold time	tRSH	ns	60		75		100	1V0 = 190	2000
CAS precharge time (Page cycle)	tCP	ns	60		60		80	Laiskage	Tax certain
CAS pulse width	tCAS	ns	60	10,000	75	10,000	100	10,000	osto i
CAS hold time	tCSH	ns	120		150		200	E Z TUO	12V
RAS to CAS delay time	tRCD	ns	25	60	25	75	30	100	7
CAS to RAS precharge time	tCRP	ns	0	TOA	0	m S.D. =	0	stov wol	DOD L
Row Address set-up time	tASR	ns	0	diam's house	0		0		
Row Address hold time	tRAH	ns	20		20		25		
Column Address set-up time	tASC	ns	0		0		0		
Column Address hold time	tCAH	ns	20		20		25	PMATI	JAT
Column Address hold time referenced to RAS	tAR	ns	80	a	95	71	125	q	
Read command set-up time	tRCS	ns	0		0	reA - a	0	ut Capadit	avit
Read command hold time	tRCH	ns	0		0	AS, CAS	0	ur Capacit	anl
Write command set-up time	twcs	ns	-10	9	-10	(TUOO)	-10	tput Capes	8
Write command hold time	twch	ns	40	. nameli	45	d with B	55	n barretine	
Write command hold time referenced to RAS	tWCR	ns	100		120		155		
Write command pulse width	twp	ns	40		45		55		
Write command to RAS lead time	tRWL	ns	40		45		55		
Write command to CAS lead time	tCWL	ns	40		45		55		
Data-in set-up time	tDS	ns	0		0		0		
Data-in hold time	tDH	ns	40		45		55		
Data-in hold time referenced to RAS	tDHR	ns	100		120		155		
CAS to WE delay	tCWD	ns	40		45		55		8
RAS to WE delay	tRWD	ns	100		120		155		8
Read command hold time referenced to RAS	tRRH.	ns	0		0		0		
CAS precharge time	tCPN	ns	30		35		45		

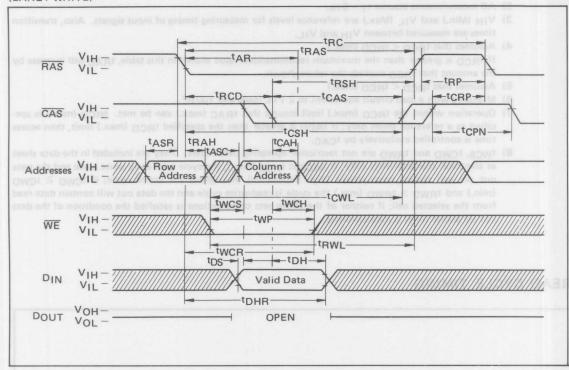
- NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Examples; RAS only) before proper device operation is achieved.
 - 2) AC measurements assume t_T = 5 ns.
 - 3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
 - 4) Assumes that t_{RCD} < t_{RCD} (max.).
 If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
 - 5) Assumes that tRCD < tRCD (max.)
 - 6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 - 7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
 - 8) twcs, tcwp and trwp are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if twcs ≥ twcs (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tcwp ≥ tcwp (min.) and trwp > trwp (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

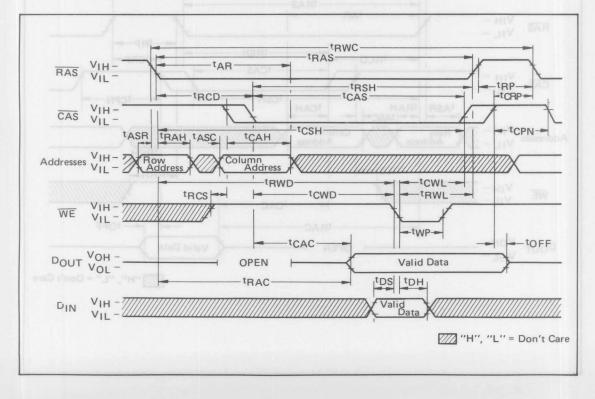


WRITE CYCLE TIMING

(EARLY WRITE)



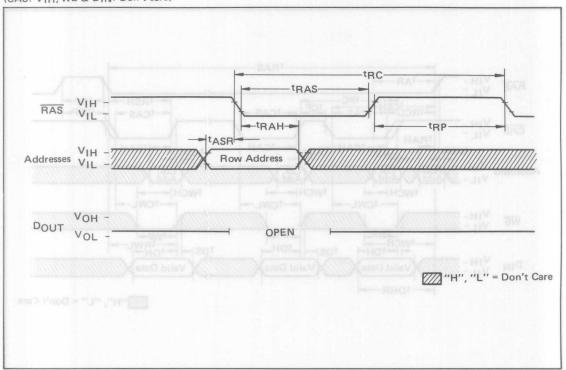
READ-WRITE/READ-MODIFY-WRITE CYCLE



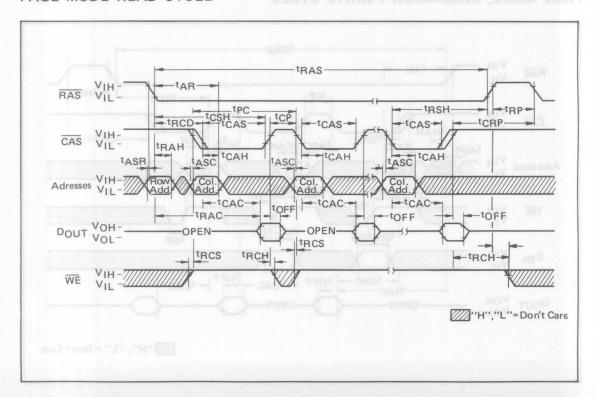
9

RAS ONLY REFRESH TIMING

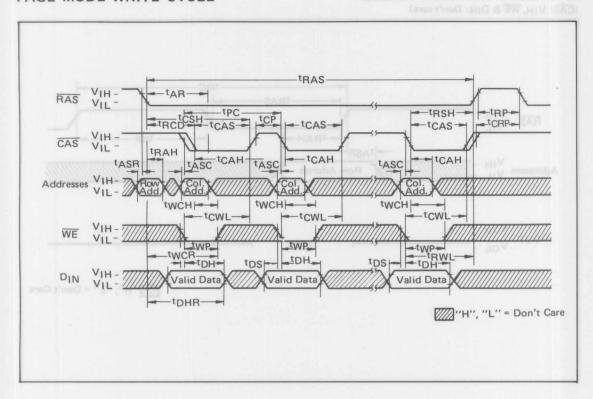
(CAS: VIH, WE & DIN: Don't care)



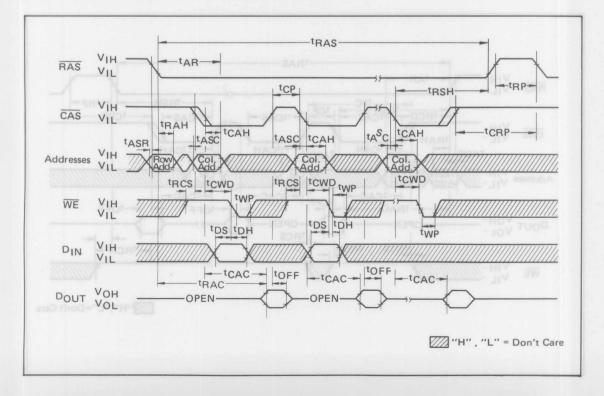
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

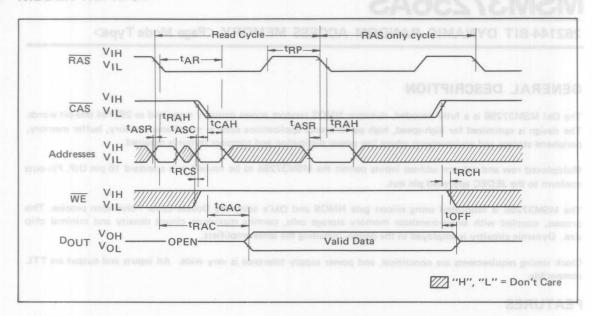


PAGE MODE, READ-MODIFY-WRITE CYCLE



9

HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764A. Eight row-address bits are established on the input pins $(A_0 \sim A_7)$ and latched with the Row Address Strobe (\overline{RAS}) . The eight column-address bits are established on the input pins and latched with the Column Address Strobe (\overline{CAS}) . All input addresses must be stable on or before the falling edge of \overline{RAS} . \overline{CAS} is internally inhibited (or "gated") by \overline{RAS} to permit triggering of \overline{CAS} as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the \overline{WE} input. A logic high (1) on \overline{WE} dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764A during a write or read-write cycle. The last falling edge of \overline{WE} or \overline{CAS} is a strobe for the Data In (D_{1N}) register. In a write cycle, if \overline{WE} is brought low (write mode) before \overline{CAS} , D_{1N} is strobed by \overline{CAS} , and the set-up and hold times are referenced to \overline{CAS} . In a read-write cycle, \overline{WE} will be delayed until \overline{CAS} has made its negative transistion. Thus D_{1N} is strobed by \overline{WE} , and set-up and hold times are referenced to \overline{WE} .

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the

same polarity as data-in. The output is in a high impedance state until \overline{CAS} is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of \overline{RAS} when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of \overline{CAS} when the transition occurs after t_{RCD} (max.). Data remain valid until \overline{CAS} is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764A while maintaining \overline{RAS} at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of \overline{RAS} is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses $(A_0\!\sim\!\!A_6)$ at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7 . RAS only refresh avoids any output during refresh because the output buffer is in the high impedance state unless \overline{CAS} is brought low. Strobing each of 128 row-addresses with \overline{RAS} will cause all bits in each rwo to be refreshed. Further \overline{RAS} -only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

RAS ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{\text{CAS}}$ as V_{IL} from a previous memory read cycle.

MSM37256AS

262144-BIT DYNAMIC RANDOM ACCESS MEMORY < Page Mode Type>

GENERAL DESCRIPTION

The Oki MSM37256 is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM37256 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MSM37256 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262144 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
 - 150 ns max (MSM37256-15AS) 200 ns max (MSM37256-20AS)
- Cycle time,
 - 270 ns min (MSM37256-15AS) 330 ns min (MSM37256-20AS)
- Low power: 440 mW active,
 28 mW max standby
- Single +5V Supply, ±10% tolerance

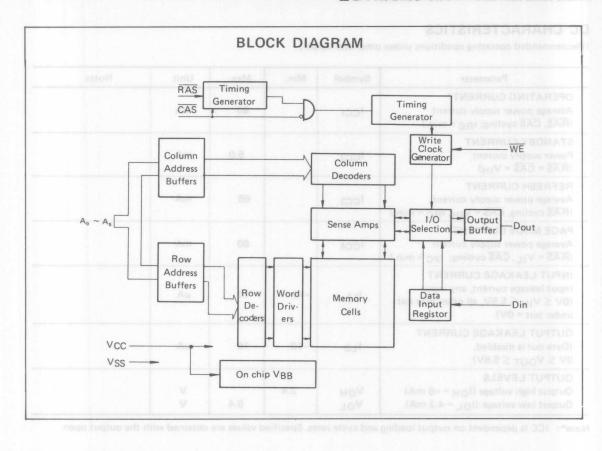
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 256 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, RAS-only refresh, and Page
 Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance

PIN CONFIGURATION



Pin Names	Function				
$A_0 \sim A_8$	Address Inputs				
RAS	Row Address Strobe				
CAS	Column Address Strobe				
WE	Write Enable				
Din	Data Input				
Dout	Data Output				
Vcc	Power (+5V)				
Vss	Ground (0V)				

* Refresh Address



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit	
Voltage on any pin relative to VSS	V _{IN} , V _{OUT}	-1 to +7		
Voltage on V _{CC} supply relative to V _{SS}	Vcc	-1 to +7	V	
Operating temperature	Topr	0 to 70	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Power dissipation	PD	1.0	W	
Short circuit output current		50	mA	

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Operating Temperature
Supply Voltage	Vcc	4.5	5.0	5.5	V	0°C to +70°C
	Vss	0	0	0	V	
Input High Voltage, all inputs	VIH	2.4		6.5	V	
Input Low Voltage, all inputs	VIL	-1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current (RAS, CAS cycling; tRC = min.)	Icc1	4	80	mA	
STANDBY CURRENT Power supply current (RAS = CAS = V _{IH})	I _{CC2}	V-	5.0	mA	
REFRESH CURRENT Average power supply current (RAS cycling, CAS = VIH; tRC = min.)	I _{CC3}		65	mA	
PAGE MODE CURRENT* Average power supply current (RAS = V _{IL} , CAS cycling; tp _C = min.)	I _{CC4}		60	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input $(0V \le V_{\text{IN}} \le 5.5V$, all other pins not under test = 0V)	VILLEM elle	-10	10	μΑ	
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \le V_{OUT} \le 5.5V$)	I _{L0}	-10	10	μА	Voc
OUTPUT LEVELS Output high voltage (IOH = -5 mA) Output low voltage (IOL = 4.2 mA)	V _{OH} V _{OL}	2.4	0.4	V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

 $(T_a = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Тур.	Max.	Unit
Input Capacitance (A ₀ ~ A ₈ , D _{IN})	CIN1	5	7	pF
Input Capacitance (RAS, CAS, WE)	C _{IN2}	7	10	pF
Output Capacitance (DOUT)	COUT	5	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS Volume and the second of the second leading and t

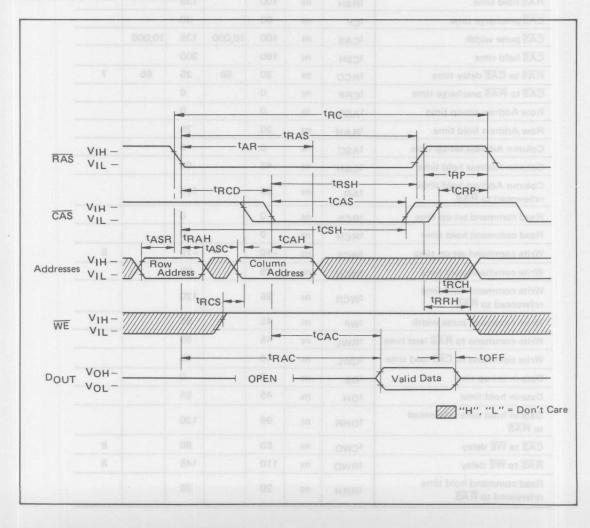
Notes 1, 2, 3 Under Recommended
Operating conditions

STORY IN THIS SEDIE, THAN ON THE	DIES DEGI	response	MSM:	37256-15	MSM:	37256-20	Dial and
Parameter	Symbol	Units	Min.	Max.	Min.	Max.	Note
Refresh period	tREF	ms	i tensin	4	lo beol	4	Moasu
Random read or write cycle time	tRC	ns	270	vine thi	330	as a refere	beilio
Read-write cycle time	tRWC	ns	270	tively by t	330	ellenines	i emij
Page mode cycle time	tPC	ns	170	John una g	225	MR CIVIOT	WCS.
Access time from RAS	tRAC	ns	rigirt)	150	o nisa	200	4,6
Access time from CAS	tCAC	ns	D B/III	100	B1 < 0	135	5,6
Output buffer turn-off delay	tOFF	ns	0	40	0	50	s) tuo
Transition time	tT	ns	3	35	3	50	
RAS precharge time	tRP	ns	100		120		
RAS pulse width	tRAS	ns	150	10,000	200	10,000	
RAS hold time	tRSH	ns	100		135	DINH INIT	31,
CAS precharge time	tCP	ns	60		80		
CAS pulse width	tCAS	ns	100	10,000	135	10,000	
CAS hold time	tCSH	ns	150		200		
RAS to CAS delay time	tRCD	ns	20	50	25	65	7
CAS to RAS precharge time	tCRP	ns	0		0		
Row Address set-up time	tASR	ns	0		0		
Row Address hold time	tRAH	ns	20		25		
Column Address set-up time	tASC	ns	0	1,6/1	0		nr [41]
Column Address hold time	tCAH	ns	45		55		-30
Column Address hold time referenced to RAS	^t AR	ns	95	GOR!	120		
Read command set-up time	tRCS	ns	0		0		HI
Read command hold time	tRCH	ns	0		0	REAL	
Write command set-up time	twcs	ns	-10	TASCT T	-10		8
Write command hold time	twcH	ns	45		55	BA M	- 11
Write command hold time referenced to RAS	twcr	ns	95		120		
Write command pulse width	tWP	ns	45	1	55		- H1/
Write command to RAS lead time	tRWL	ns	45		55		-710
Write command to CAS lead time	tCWL	ns	45		55		
Data-in set-up time	tDS	ns	0		0		-HO
Data-in hold time	tDH	ns	45		55		30
Data-in hold time referenced to RAS	tDHR	ns	95		120		
CAS to WE delay	tCWD	ns	60		80		8
RAS to WE delay	tRWD	ns	110		145		8
Read command hold time referenced to RAS	tRRH	ns	20		25		

- NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Examples; RAS only) before proper device operation is achieved.
 - 2) AC measurements assume $t_T = 5 \text{ ns.}$
 - 3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
 - 4) Assumes that t_{RCD} < t_{RCD} (max.).

 If t_{RCD} is greater than the maximum recommended val
 - If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
 - 5) Assumes that t_{RCD} < t_{RCD} (max.)
 - 6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 - 7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
 - 8) tWCS, tCWD and tRWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if tWCS ≥ tWCS (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tCWD ≥ tCWD (min.) and tRWD > tRWD (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

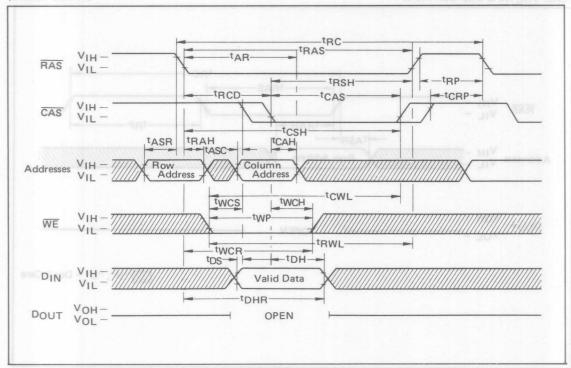
READ CYCLE TIMING



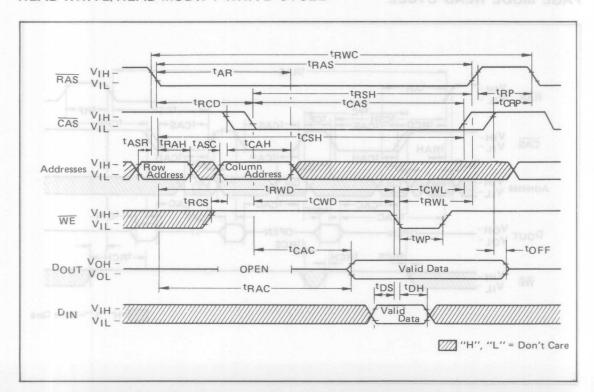
9

WRITE CYCLE TIMING

(EARLY WRITE)

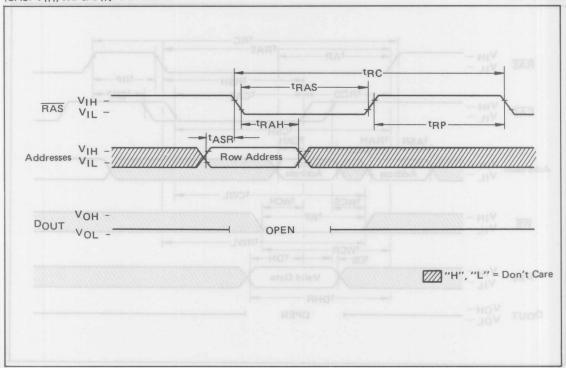


READ-WRITE/READ-MODIFY-WRITE CYCLE

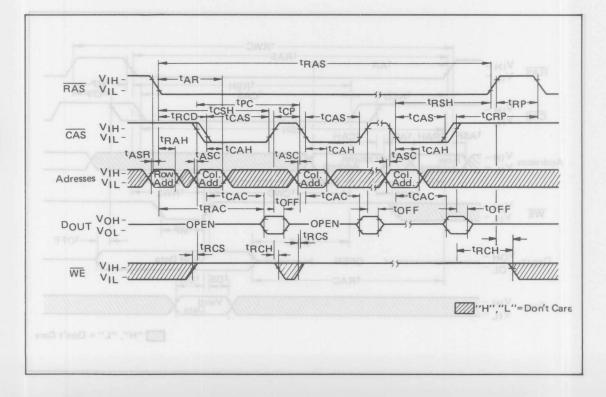


RAS ONLY REFRESH TIMING

(CAS: VIH, WE & DIN: Don't care)

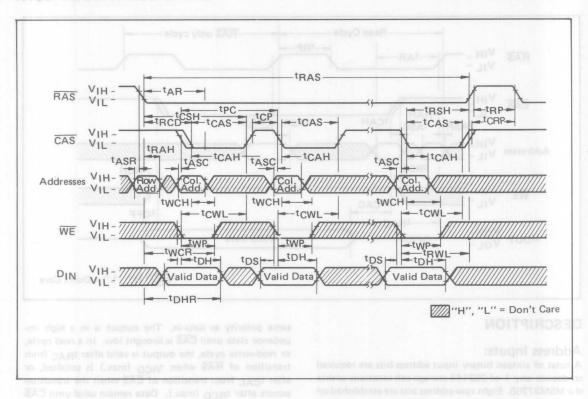


PAGE MODE READ CYCLE

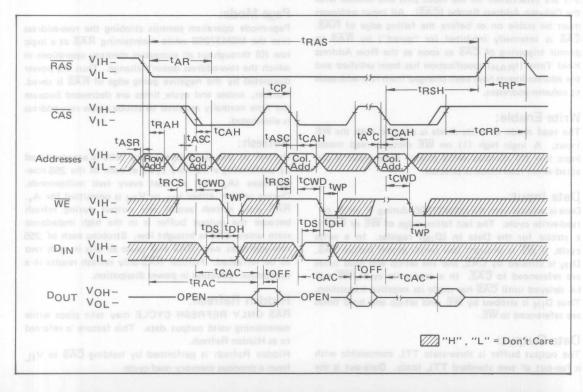


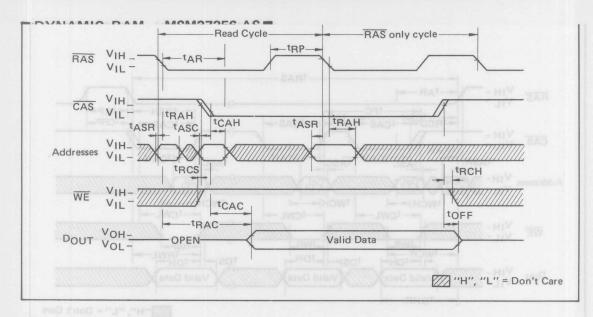
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PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE





DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 262144 storage cell locations within the MSM37256. Eight row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe (RAS). The eight column-address bits are established on the input pins and latched with the Column Address Strobe (CAS). All input addresses must be stable on or before the falling edge of RAS. CAS is internally inhibited (or "gated") by RAS to permit triggering of CAS as soon as the Row Address Hold Time (trah) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the WE input. A logic high (1) on $\overline{\text{WE}}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM37256 during a write or read-write cycle. The last falling edge of \overline{WE} or \overline{CAS} is a strobe for the Data In (DIN) register. In a write cycle, if \overline{WE} is brought low (write mode) before \overline{CAS} , DIN is strobed by \overline{CAS} , and the set-up and hold times are referenced to \overline{CAS} . In a read-write cycle, \overline{WE} will be delayed until \overline{CAS} has made its negative transistion. Thus DIN is strobed by \overline{WE} , and set-up and hold times are referenced to \overline{WE} .

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the

same polarity as data-in. The output is in a high impedance state until \overline{CAS} is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of \overline{RAS} when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of \overline{CAS} when the transition occurs after t_{RCD} (max.). Data remain valid until \overline{CAS} is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM37256 while maintaining RAS at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of RAS is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8 . \overline{RAS} only refresh avoids any output during refresh because the output buffer is in the high impedance state unless \overline{CAS} is brought low. Strobing each of 256 row-addresses with \overline{RAS} will cause all bits in each rwo to be refreshed. Further \overline{RAS} -only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

RAS ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{\text{CAS}}$ as V_{IL} from a previous memory read cycle.

MSM41256AS/RS

262144-BIT DYNAMIC RANDOM ACCESS EMMORY < Nibble Mode Type >

GENERAL DESCRIPTION

The Oki MSM41256 is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41256 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "CAS-before-RAS" refresh provides an on-chip refresh capability, also features "nibble mode" which allows high speed serial access to up to 4 bits of data.

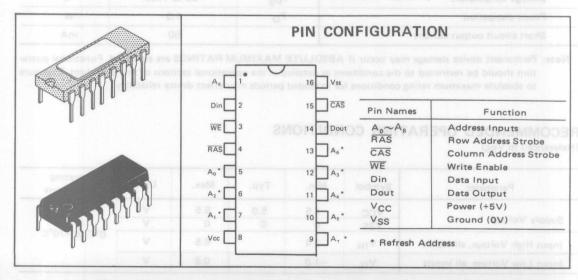
The MSM41256 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

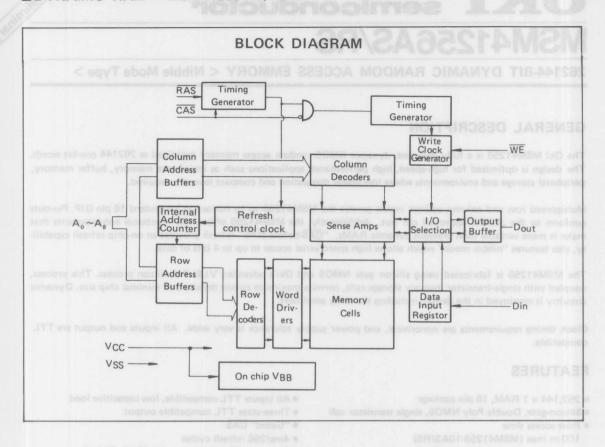
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262,144 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time
 - 100 ns max (MSM41256-10AS/RS)
 - 120 ns max (MSM41256-12AS/RS)
- 150 ns max (MSM41256-15AS/RS)
- Cycle time,
 - 200 ns min (MSM41256-10AS/RS)
- 230 ns min (MSM41256-12AS/RS) 280 ns min (MSM41256-15AS/RS)
- Low power: 415 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance

- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 4ms/256 refresh cycles
- Common I/O capability using "Early Write"
 Operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, RAS-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- CAS-before-RAS refresh capability
- · "Nibble Mode" capability





ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to VSS	V _{IN} , V _{OUT}	-1 to +7	4M2M) V m an 089
Voltage on V _{CC} supply relative to V _{SS}	Vcc	-1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Power dissipation	PD	1.0	W
Short circuit output current	MIA	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Operating Temperature
Power (+5V)	VCC	4.5	5.0	5.5	V	A POST OF THE
Supply Voltage	Vss	0	0	0	V	
Input High Voltage, all inputs	VIH	2.4		6.5	V	0°C to +70°C
Input Low Voltage, all inputs	VIL	-1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current (RAS, CAS cycling; tRC = min.)	I _{CC1}	MSM	75	mA	Parameter
STANDBY CURRENT Power supply current (RAS = CAS = VIH)	I _{CC2}	19 s 200	5.0	mA	Refresh period
REFRESH CURRENT Average power supply current (RAS cycling, CAS = VIH; tRC = min.)	I _{CC3}	g 245 s 150	60	mA	Read-write cycle time Page mode cycle time
Nibble MODE CURRENT* Average power supply current (RAS = V _{IL} , CAS cycling; tpc = min.)	ICC4	2 2	- Unit	mA	Access time from RAS Access time from CAS
INPUT LEAKAGE CURRENT Input leakage current, any input $(0V \le V_{\mbox{IN}} \le 5.5V$, all other pins not under test = 0V)	35 ILI 10,000	-10	10	μА	Transition time A.S. precharge time 3.A.S. outer width
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V)$	lLO	-10	10	μА	RAS hold Gare CAS pulse width
OUTPUT LEVELS Output high voltage (IOH = -5 mA) Output low voltage (IOL = 4.2 mA)	VOH VOL	2.4	/ / / / /	V	CAS hold time. RAS to CAS delay time

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

 $(T_a = 25^{\circ} C, f = 1 MHz)$

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A ₀ ~ A ₈ , D _{IN})	CIN1	5	7	pF
Input Capacitance (RAS, CAS, WE)	C _{IN2}	7	10	pF
Output Capacitance (DOUT)	COUT	5	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended
Operating conditions

Parameter Am	76	Linite	MSM4	1256-10	MSM4	1256-12	MSM	MSM41256-15	
Parameter	Symbol	Units	Min.	Max.	Min.	Max.	Min.	Max.	Note
Refresh period	tREF .	ms		4		4	199	4	ANDS
Random read or write cycle time	tRC	ns	200		230		280	MV = ZAI	- EA
Read-write cycle time	tRWC	ns	245		280		335	H CURRE	ERES
Page mode cycle time	tPC	ns	150	1003	170	ine	225	sower supp	again
Access time from RAS	tRAC	ns		100	1	120	September 1	150	4,6
Access time from CAS	tCAC	ns		50		60	nua yk	75	5, 6
Output buffer turn-off delay	tOFF	ns	0	25	0	25	0	30	= 88
Transition time	tŢ	ns	3	35	3	35	3	50	TUR
RAS precharge time	tRP	ns	90	111	100	on anic you	120	VA2 > IA	1011 7 U.S
RAS pulse width	tRAS	ns	100	10,000	120	10,000	150	10,000	st rab
RAS hold time	tRSH	ns	50		60	TIMBRI	75	LEAKAG	TPUT
CAS pulse width	tCAS	ns	50	10,000	60	10,000	75	10,000	10 am
CAS hold time	tCSH	ns	100		120		150	212021	T LEVY
RAS to CAS delay time	tRCD	ns	20	50	25	60	25	75	7
CAS to RAS precharge time	tCRP	ns	0	JOY	0	64.2 mAt	0	opstiov wo	Bigh
Row Address set-up time	tASR	ns	0	nd cycle n	0	output lo	0	la depined	101
Row Address hold time	tRAH	ns	15		20		20		
Column Address set-up time	tASC	ns	0		0		0	TAME	PAR
Column Address hold time	tCAH	ns	15		20		20	HMT=1,	25°C
Column Address hold time referenced to RAS	tAR	ns	65	nya	85		95	119	
Read command set-up time	tRCS	ns	0	RP	0	14-18A -	0	relicação i	Inpu
Read command hold time	tRCH	ns	0	139	0	US, CAS, V	0	(Capacitai	Inpu
Write command set-up time	twcs	ns	0	99	0	TTUO	0	neqs3 tu	8
Write command hold time	twch	ns	40	.nate	45	with 8oo	50	en sanstin	Cap
Write command hold time referenced to RAS	twcr	ns	80		95		120		
Write command pulse width	twp	ns	20		25		30		
Write command to RAS lead time	tRWL	ns	40		45		50		
Write command to CAS lead time	tCWL	ns	40		45		50		
Data-in set-up time	tDS	ns	0	1	0		0		
Data-in hold time	tDH	ns	20		25		30		
Data-in hold time referenced to RAS	tDHR	ns	70		85		105		
CAS to WE delay	tCWD	ns	50		60		75		8
RAS to WE delay	tRWD	ns	100		120		150		8
Read command hold time referenced to RAS	tRRH	ns	20		20		25		

AC CARACTERISTICS (Continued)

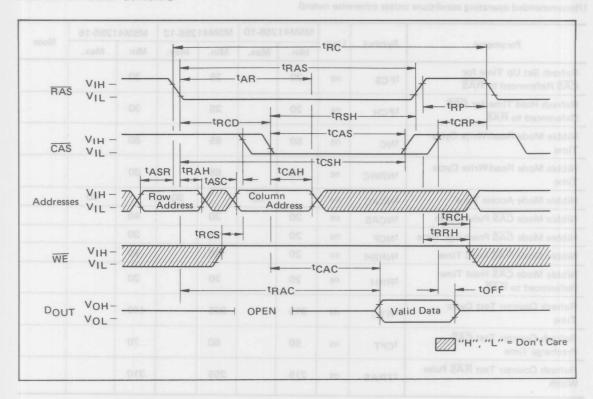
(Recommended operating conditions unless otherwise noted)

			MSM4	256-10	MSM41	1256-12	MSM4	1256-15	
Parameter	Symbol	Unit	Min.	Max.	Min.	Max.	Min	Max.	Note
Refresh Set Up Time for CAS Referenced to RAS	tFCS	ns	20	RA	25		30	- seV	
Refresh Hold Time for CAS Referenced to RAS	tFCH	ns	20		25		30	- 71A	
Nibble Mode Read/Write Cycle Time	tNC	ns	50	D	65		80	- HIV	AS
Nibble Mode Read-Write Cycle Time	tNRWC	ns	50		65	ARI SE	80		
Nibble Mode Access Time	tNCAC	ns	(assault	20	XUDX	30	F X	40	menbbs
Nibble Mode CAS Pulse Width	tNCAS	ns	20		30		40	-114	
Nibble Mode CAS Precharge Time	tNCP	ns	20		25		30		
Nibble Mode RAS Hold Time	tNRSH	ns	20		30		40	- HIIV	100
Nibble Mode CAS Hold Time Referenced to RAS	^t RNH	ns	20		20		20	-11%	
Refresh Counter Test Cycle Time	^t RTC	ns	315	огви	365		440	-HOV T	upe
Refresh Counter Test CAS Precharge Time	tCPT	ns	50		60		70		
Refresh Counter Test RAS Pulse Width	tTRAS	ns	215		255		310		

NOTES: 1) An initial pause of $100 \,\mu s$ is required after power-up followed by any 8 \overline{RAS} cycles (Examples; \overline{RAS} only) before proper device operation is achieved.

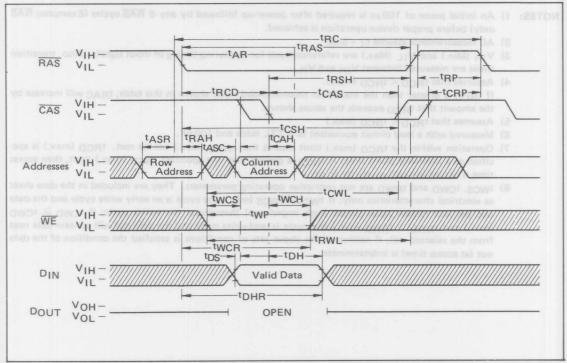
- 2) AC measurements assume $t_T = 5 \text{ ns.}$
- 3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- 4) Assumes that t_{RCD} < t_{RCD} (max.).
 - If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the values shown.
- 5) Assumes that tRCD < tRCD (max.)
- 6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
- 7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
- 8) twcs, tcwp and trwp are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if twcs ≥ twcs (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tcwp ≥ tcwp (min.) and trwp > trwp (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

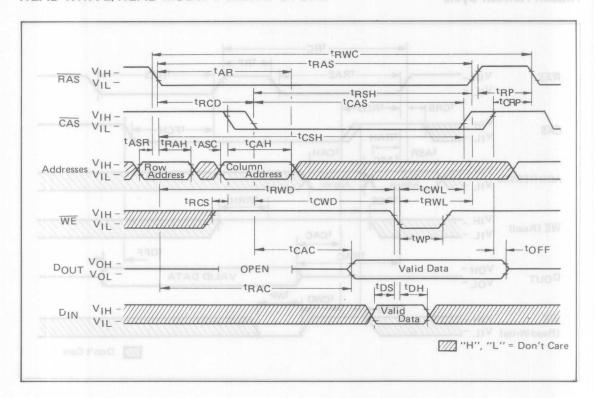


WRITE CYCLE TIMING

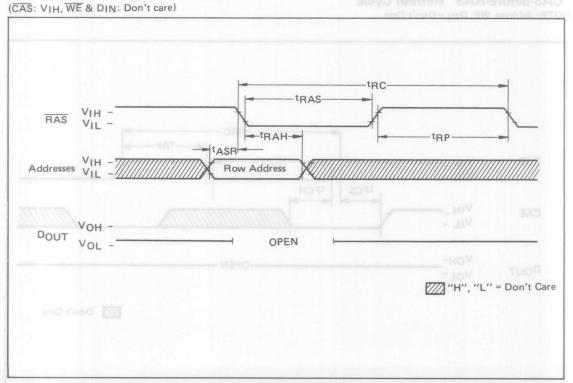
(EARLY WRITE)



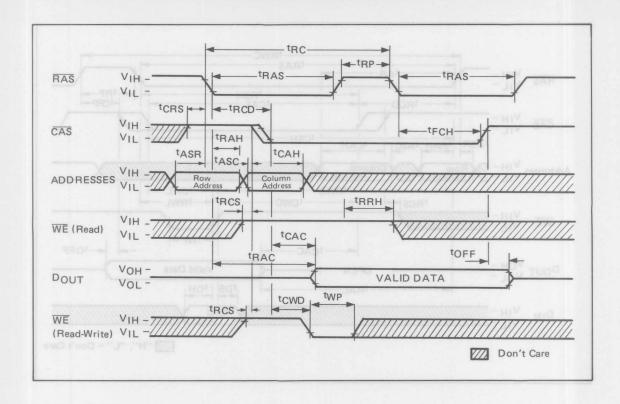
READ-WRITE/READ-MODIFY-WRITE CYCLE



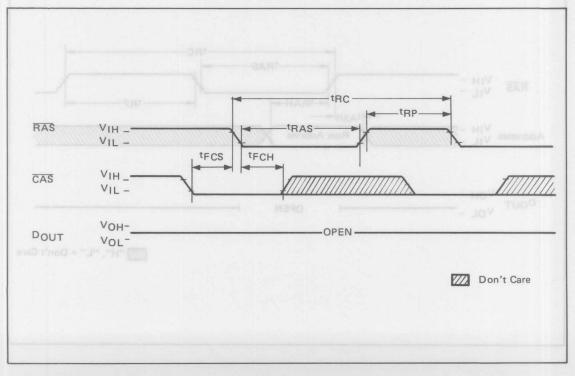
RAS ONLY REFRESH TIMING



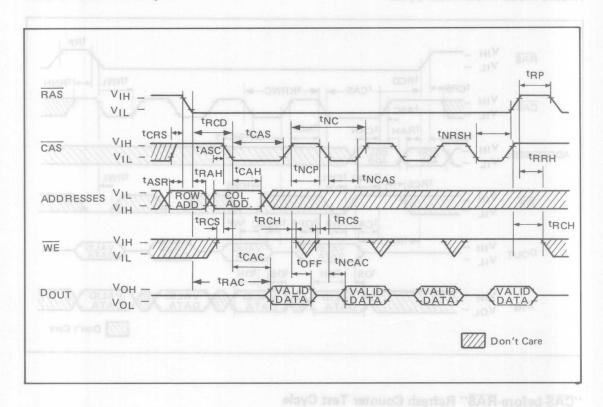




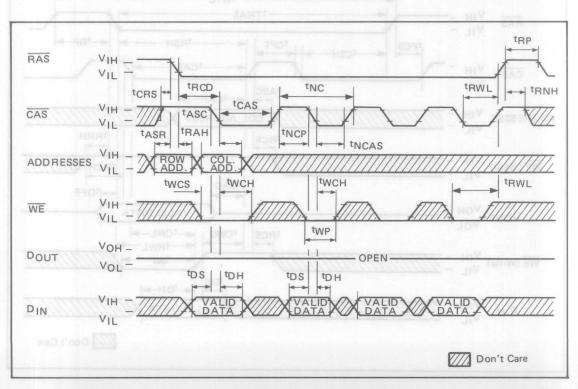
"CAS-before-RAS" Refresh Cycle NOTE: Address, WE, DIN = Don't Care



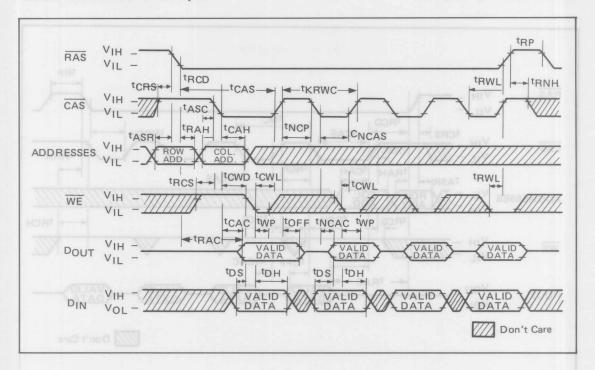
Nibble Mode Read Cycle



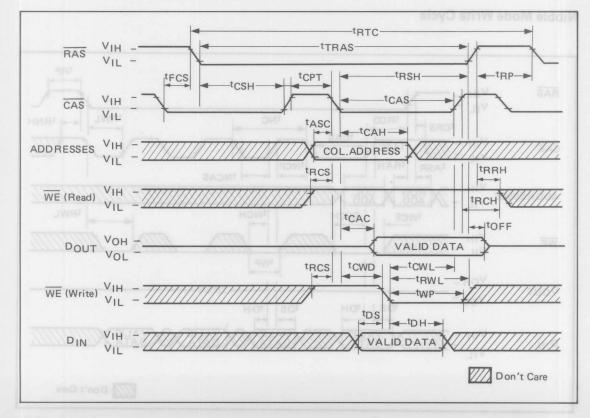
Nibble Mode Write Cycle



Nibble Mode Read-Write Cycle



"CAS-before-RAS" Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement

The MSM41256 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41256 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM41256 has the minimal hold times of Address (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). And the MSM41256 can commit better memory system through-put during operations in an inter-leaved system. Furthermore, Oki has made timing requirements referenced to \overline{RAS} non-restrictive and deleted from the data sheet, which includes t_{AR} , t_{WCR} , t_{DHR} and t_{RWD} . Therefore,the hold times of the Column Address, Din and \overline{WE} as well as t_{CWD} (\overline{CAS} to \overline{WE} Delay) are not ristricted by t_{RCD} .

Fast Read- While-Write cycle

The MSM41256 has the fast read while write cycle which is achieved by excellent control of the Tri-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of \overline{WE} when \overline{CAS} goes low. When \overline{WE} is low during \overline{CAS} transition to low, the MSM41256 goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when \overline{WE} goes low after tCWD following \overline{CAS} transition to low, the MSM41256 goes to delayed write mode where the output contains the data from the cell selected and the data from Din is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs

A total of eighteenbinary input address bits are required to decode any 1 of 262144 cell locations within MSM41256. Nine row-address bits are established on the input pins (A $_0$ through A $_8$) and latched with the Row Address Strobe (\overline{RAS}). Then nine column address bits are established on the input pins and latched with the Column Address Strobe (\overline{CAS}). All input addresses must be stable on or before the falling edge of \overline{RAS} . \overline{CAS} is internally inhibited (or "gated") by \overline{RAS} to permit triggering of \overline{CAS} as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read or write mode is selected with the \overline{WE} input. A logic "high" on \overline{WE} dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MSM41256 during a write or read-write cycle. The last falling edge of \overline{WE} or \overline{CAS} strobes the Data In (D_{IN}). In a write cycle, if \overline{WE} is brought "low" (write mode) before \overline{CAS} , D_{IN} is strobed by \overline{CAS} , and the set-up and hold times are referenced to \overline{CAS} . In a read-write cycle, \overline{WE} will be delayed until \overline{CAS} has made its negative transition. Thus D_{IN} is storbed by \overline{WE} , and set-up and hold times are referenced to \overline{WE} .

Data Output

The output byffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until \overline{CAS} is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transistion of \overline{RAS} when $t_{RCD}(max)$ is satisfied, or after t_{CAC} from transition of \overline{CAS} when the transition occurs after t_{RCD} (max) Data remains valid until \overline{CAS} is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode

Nibble mode allows high speed serial read, write or readmodify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA₈ RA₈) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by CAS "high" then "low" while RAS remains "low". Toggling CAS causes RA₈ and CA₈ to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation may be executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the tri-state control of $\mathsf{D}_{\mathsf{OUT}}$ Pin is determined by the first normal access cycle.

The data output is controlled by only \overline{WE} state referenced at \overline{CAS} negative transition of the normal cycle (Nibble first bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain open circuit throughout the succeeding Nibble cycle regardless to \overline{WE} state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during regardless to \overline{WE} state. The write operation is done during the period where \overline{WE} and \overline{CAS} clocks are low. Therefore, write operation can be done bit by bit during each nibble operation at any timing conditions of \overline{WE} (t_{WCS} and t_{CWD}) at the normal cycle (nibble first bit).

	NIBBLE	BIT	ROW ADDRESS	andly		
SEQUENCE		RA ₈		CA ₈		
RAS/CAS (normal mode)	1	0	10101010	0	101010 10	input addresses
toggle CAS (nibble mode)	2	1	10101010	0	101010 10	continual time space for (id
toggle CAS (nibble mode)	3	0	10101010	in 1 and	101010 10	generated inter-
toggle CAS (nibble mode)	4	1	10101010	1	101010 10	nally
toggle CAS (nibble mode)	1	0	10101010	0	101010 10	sequence repeats

NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

RAS only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 through A_1) at least every 4 ms. \overline{RAS} only refresh avoids any output during refresh because the buffer is in the high impedance state unless \overline{CAS} is brought "low". Strobing each of the 256 row-addresses (A_0 through A_1) with \overline{RAS} will cause all bits in each row to be refreshed. Further \overline{RAS} only refresh results in a substantial reduction in power dissipation.

CAS before RAS Refresh

 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on MSM41256 offers an alternate refresh method. If $\overline{\text{CAS}}$ is held on "low" for the specified period (tFCS) before $\overline{\text{RAS}}$ goes to "low", on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ befoe $\overline{\text{RAS}}$ refresh operation.

Hidden Refresh

Hidden refresh cycle may takes place while maintaining latest valid data at the output by extending \overline{CAS} active time. In MSM41256 hidden refresh means \overline{CAS} before \overline{RAS} refresh and the internal refresh addresses from the counter are used to refresh addresses, because \overline{CAS} is always "low" when \overline{RAS} goes to "low" in hidden refresh.

CAS before RAS Refresh Counter Test

A special timing sequence using \overline{CAS} before \overline{RAS} counter test cycle provides a convenient method of verifying the functionality of \overline{CAS} before \overline{RAS} refresh activted circuitry.

As shown in \overline{CAS} before \overline{RAS} Counter Test Cycle, after the \overline{CAS} before \overline{RAS} refresh operation, if \overline{CAS} goes to "high" and goes to "low" again while \overline{RAS} is held "low", the read and write operation are enabled. A memory cell address (consisting of a row address (9 bits) and a column address (9 bits)) to be accessed can be defined as follows:

- * A ROW ADDRESS Bits A₀ through A₇ are defined by the refresh counter.
- The other bit A₈ is set "high" internally.
- * A COLUMN ADDRESS All the bits A₀ through A₈ are defined by latching levels on A₀ through A₈ at the second falling edge of CAS.

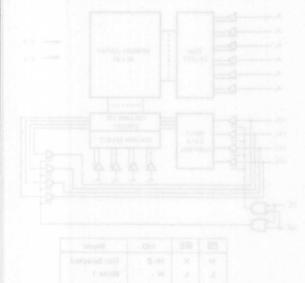
SUGGESTED CAS before RAS COUNTER TEST PROCEDURE

The timing as shown in CAS before RAS Counter Test Cycle is used for all the operations described as follows:

- (1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
- (2) Write a test pattern of "low"s into memory cells at a single column address and 256 row addresses.
- (3) By using read-modify-write cycle, read the "low" written at the last operation (Step (2)) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.
- (4) Read the "high"s written at the last operation (Step (3)).
- (5) Compliment the test pattern and repeat the steps (2), (3) and (4).

MOS

STATIC **RAMS**





MSM2114LRS

4096-BIT (1024 x 4) STATIC RAM (E3-S-006-32)

GENERAL DESCRIPTION

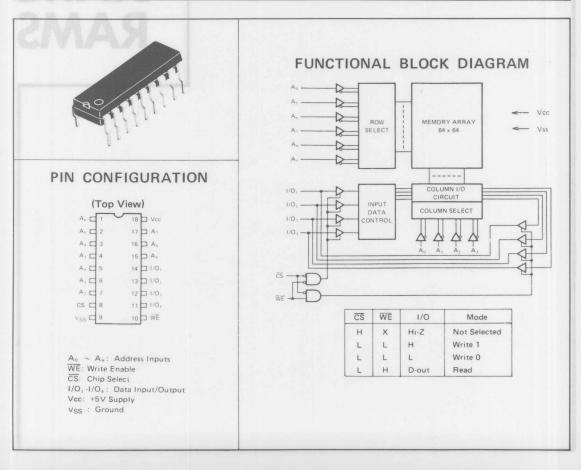
The Oki MSM2114L is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable N-channel Silicon Gate MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Directly TTL compatible inputs, outputs and operation from a single +5V supply simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM2114L series is offered in an 18-pin dual-in-line plastic (RS Suffix) package. The series is guaranteed for operation from 0°C to 70°C.

FEATURES

- Low Power Dissipation
- High Density 300-mil 18-Pin Package
- Fully Static Operation
- Three-State Outputs
- Directly TTL Compatible
- Single +5V Supply (±10% Tolerance) Common I/O Capability using N-channel Silicon Gate MOS Technology
 - Interchangeable with Intel 2114L Devices

	2114L-2	2114L-3	2114L
Max. Access Time (NS)	200	300	450
Max. Power Dissipation (MW)	396	396	396



y

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Temperature Under Bias	Topr	0 to +70	°C	
Storage Temperature	T _{stg}	-55 to +150	°C	Parami
Supply Voltage	Vcc	-0.5 to +7	V	
Input Voltage	VIN	-0.5 to +7	V	Respect to VSS
Output Voltage	Vout	-0.5 to +7	V	emi FatagoA
Power Dissipation	PD	1.0	W	bileV

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

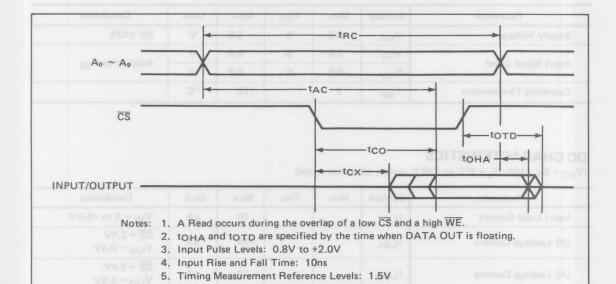
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Supply Voltage	Vcc	4.5	5	5.5	V	5V ±10%	
	VIH	2.0	5	6.0	V	Respect to V _{SS}	
Input Signal Level	VIL	-0.5	0	0.8	V		
Operating Temperature	Topr	0		+70	°C		

DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%, T_a = 0^{\circ}C \text{ to } +70^{\circ}C, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
nput Load Current	JLI	s to only	ovo artr soi	10	μΑ	V _{IN} = 0 to +5.5V
/O Leakage Current	ILOL	thy the till 2.0V		-10	μΑ	$\overline{CS} = 2.4V$ $V_{1/O} = 0.4V$
/O Leakage Current	ILOH	ns ce Levels:	nt liteteres	10	μΑ	$\overline{CS} = 2.4V$ $V_{1/O} = 5.5V$
Output High Voltage	Voh	2.4		Vcc	V	$I_{OH} = -0.2mA$
Output Low Voltage	VoL			0.4	V	I _{OL} = 2.0mA
Power Supply Current	lcc		21146-218	72	mA	$V_{CC} = 5.5V$ $I/O = 0mA$ $T_{\Delta} = 0^{\circ}C$

0	0 -1 -1	2114	L-2RS	2114	L-3RS	211	4LRS	
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	tRC	200		300		450	Service Ass	ns
Access Time	tAC		200	8/11	300		450	ns
Chip Selection to Output Valid	tco	1.0	70	a ^r	100	no	120	ns
Chip Selection to Output Active	tcx	20	HIXAM 3	20	ed upder ting only	20	ses shows se, This is	ns
Output 3-state from Deselection	totd	ilisega ali Nect devil	60	rez lenois; reti babre	80	dicared in	100	ns
Output Hold from Address Change	toha	10		10		10		ns



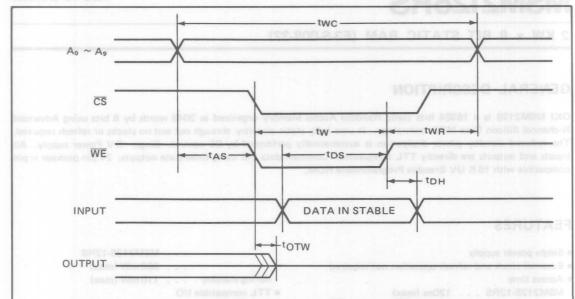
6. Output Load: 1 TTL Gate and CL = 50pF

WRITE CYCLE

 $(V_{CC} = 5V \pm 10\%, T_a = 0^{\circ}C \text{ to } 70^{\circ}C)$

TAPOC		2114	L-2RS	2114	L-3RS	211	4LRS	
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle Time	twc	200		300		450		ns
Write Time	tw	120	45.	150		200		ns
Write Release Time	twR	20		30		50		ns
Address Setup Time	t _{AS}	0		0		0		ns
Data Setup Time	t _{DS}	120		150		200		ns
Data Hold From Write Time	t _{DH}	0		0		0		ns
Write Enabled to Output in High Z	toTW		60		80		100	ns

WRITE CYCLE



Notes: 1. A Write occurs during the overlap of a low \(\overlap \) and a low \(\overlap \).

- 2. Input Pulse Levels: 0.8V to +2.0V
- 3. Input Rise and Fall Time: 10ns
- 4. Timing Measurement Reference Levels: 1.5V
 - 5. tw: Overlap time of a low CS and low WE
 - 6. tas is specified from CS or WE, whichever occurs last.
 - 7. twp, tps and tph are specified from CS or WE, whichever occurs first.
 - 8. toTW is specified by the time when DATA OUT is floating, not defined by output level.
 - 9. When I/O pins are Data output mode, don't force inverse signal to those pins.

CAPACITANCE

 $(T_a = 25^{\circ}C, f = 1MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	C _{1/O}		6	8	pF
Input Capacitance	CIN		4	6	pF

Note: This parameter is periodically sampled and not 100% tested.



MSM2128RS

2 KW x 8 BIT STATIC RAM (E3-S-008-32)

GENERAL DESCRIPTION

OKI MSM2128 is a 16384 bits static Random Access Memory organized as 2048 words by 8 bits using Advanced N-channel Silicon Gate MOS technology. It uses fully static circuitry through out and no clocks or refresh required. The reduced standby power dissipation is automatically performed by CS control. Single +5 V Power supply. All inputs and outputs are directly TTL compatible. Common data I/O using three-state outputs. 24 pin package is pin compatible with 16 K UV Erasable Programmable ROM.

FEATURES

- Single power supply
- External clock and refresh operation not required
- Access time

MSM2128-12RS . . . 120ns (max)
MSM2128-15RS . . . 150ns (max)
MSM2128-20RS . . . 200ns (max)

Low power dissipation

during operation . . . MSM2128-15RS/20RS

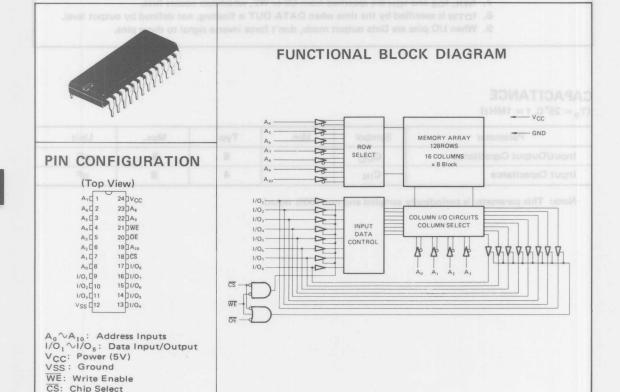
. . . 550 mW (max)

. . . MSM2128-12RS

... 660 mW (max)

during standby . . . 110 mW (max)

- TTL compatible I/O
- Three-state I/O
- Common data I/O capability
- Power down mode using chip select signal
- Convertibility of pins used in 16KEPROM MSM2716



9

OE: Output Enable

9

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V _{cc}	-0.5 to 7	V	Bearage to V
Input Voltage	VIN	-0.5 to 7	V	Respect to V _{SS}
Operating Temperature	Topr	0 to 70	°C	ddress Access Time
Storage Temperature	T _{stg}	-55 to 150	°C	orput Enable to
Power Dissipation	PD	1.0	W	Asiac melte

DC AND OPERATING CHARACTERISTICS

 $(T_a = 0^{\circ} C \text{ to} + 70^{\circ} C, V_{CC} = 5V \pm 10\%, \text{ unless otherwise notes.})$

Parameter	0	2	128-12R	S	21	28-15/2	ORS	Hais	Conditions
Parameter	Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Conditions
Input Load Current	60 TLT 08	-10	-08	10	-10		10	μА	V _{CC} = Max. V _{IN} = GND to V _{CC}
Output Leakage Current	ILO	-10		10	-10		10	μΑ	$\overline{CS} = \overline{OE} = V_{IH},$ $V_{cc} = Max.$ $V_{out} = GND \text{ to } V_{cc}$
Operating Current	Icc			120			100	mA	$V_{CC} = Max. \overline{CS} = V_{IL}$ $II/O = 0 \text{ mA } t_{CYC} = Min.$
Standby Current	I _{SB}			15			15	mA	$\frac{V_{CC}}{CS} = Min. \text{ to Max.}$
Peak Power-on Current	I _{SBP}	N		20		02	20	mA	V_{CC} = GND to V_{CC} = Min. \overline{CS} = Lower of V_{CC} or V_{IH}
-AHO	VIH	2	5	6	2	5	6	V	Decreed to V
Input Voltage	VIL	-0.5	0	0.8	-0.5	0	0.8	V	Respect to Vss
Output Voltage	Voн	2.4		V _{cc}	2.4		V _{cc}	V	I _{OH} = -1.0 mA
Output Voltage	VOL			0.4			0.4	V	I _{OL} = 2.1 mA

Notes 1. Typical limits are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$, and specified loading.

AC CHARACTERISTICS

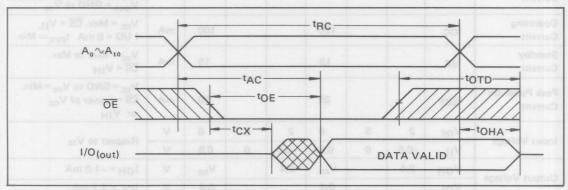
 $(T_a = 0^{\circ} C \text{ to} + 70^{\circ} C, V_{CC} = 5V \pm 10\%, \text{ unless otherwise noted.})$

AC TEST CONDITIONS

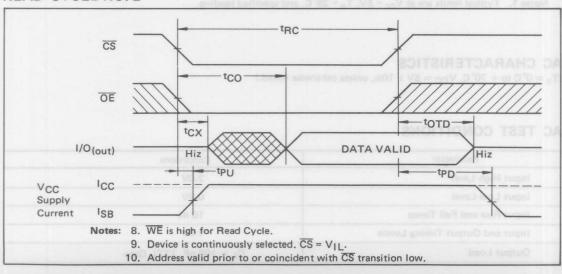
Parameter	Conditions
Input High Level	2.0V
Input Low Level	0.8V
Input Rise and Fall Times	10 ns 83 manu0
Input and Output Timing Levels	ASSOCIATION OF THE PROPERTY OF
Output Load	C _L = 100 pF, 1TTL Gate

Parameter	Combal	2128	12RS	2128	1-15RS	2128	3-20RS	Unit	Conditions
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Conditions
Read Cycle Time	tRC	120	-0.6	150	uV.	200		ns	oV zugnt
Address Access Time	tAC	70	120	1	150		200	ns	павнядО
Output Enable to Output Delay	tOE	150	50		60		70	ns	Storage
Chip Select Access Time	tco		120		150		200	ns	
Chip Selection to Output in Low Z	tcx ⁽²⁾	10		10		10		ns	
Chip Selection to Output in High Z	tOTD(3)	0	40	0	50	0	60	ns	O GND O
Output Hold from Address Time	tOHA	10	1.893	10	3D 82001	10	A0 = 3	ns	+ 0, 5 0 1 4
Chip Select to Power Up Time	tpU	0	2128- in. T	0	PIZAS	0	M lod	ns	verteren of
Chip Select to Power Down Time	tPD		50	- 01	60	0	80	ns	Input Load Curent

READ CYCLE NO. 1(8)(9)



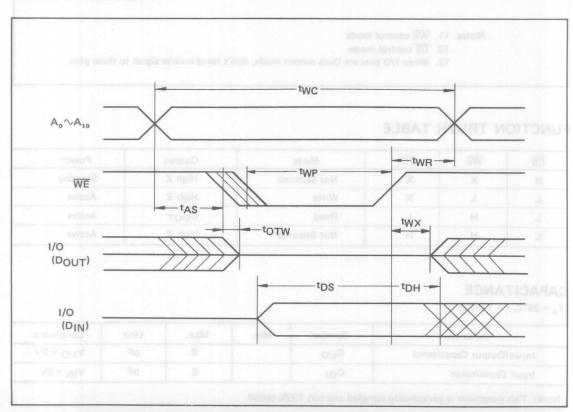
READ CYCLE NO. 2^{(8) (10)}



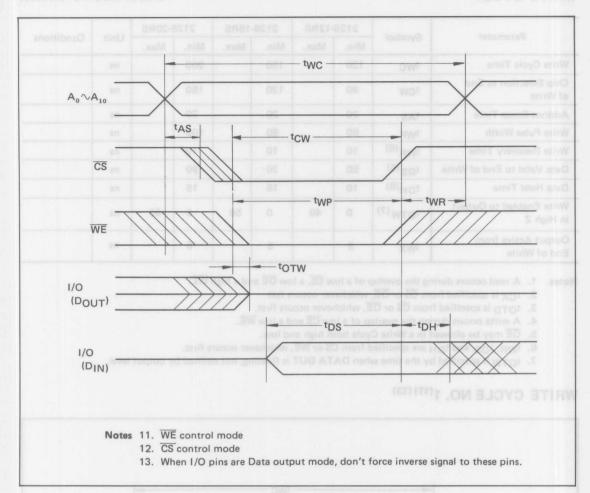
Parameter	Cumbal	2128	3-12RS	2128	3-15RS	212	8-20RS	11-14	0
rarameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Conditions
Write Cycle Time	twc	120	- OWI	150		200		ns	
Chip Selection to End of Write	tCW	90		120		150	/	ns	w.A
Address Setup Time	tAS	20		20		20		ns	
Write Pulse Width	twp	60	16/	80		100		ns	
Write Recovery Time	tWR (6)	10		10		10		ns	
Data Valid to End of Write	t _{DS} (6)	50		70	1//	90		ns	
Data Hold Time	tDH(6)	10		15		15		ns	
Write Enabled to Output in High Z	tOTW (7)	0	40	0	50	0	60	ns	
Output Active from End of White	twx	5		5	44	5	44	ns	

- Notes 1. A read occurs during the overlap of a low $\overline{\text{CS}}$, a low $\overline{\text{OE}}$ and a high $\overline{\text{WE}}$.
 - 2. tCX is specified from CS or OE, whichever occurs last.
 - 3. toTD is specified from $\overline{\text{CS}}$ or $\overline{\text{OE}}$, whichever occurs first.
 - 4. A write occurs during the overlap of a low CS and a low WE.
 - 5. OE may be allowed in a Write Cycle both high and low.
 - 6. tWR, tDS, and tDH are specified from CS or WE, whichever occurs first.
 - 7. toTW is specified by the time when DATA OUT is floating, not defined by output level.

WRITE CYCLE NO. 1(11)(13)



WRITE CYCLE NO. 2(12) (13)



FUNCTION TRUTH TABLE

CS	WE	ŌE	Mode	Output	Power	
Н	X	X	Not Selected	High Z	Standby	
L	L	X	Write	High Z	Active	
L	Н	L	Read	DOUT	Active	
L	Н	Н	Not Selected	High Z	Active	

CAPACITANCE

 $(T_a = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Min.	Max.	Unit	Conditions
Input/Output Capacitance	C _{I/O}		8	pF	V _{I/O} = 0V
Input Capacitance	CIN		6	pF	V _{IN} = 0V

Note: This parameter is periodically sampled and not 100% tested.

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OKI semiconductor

MSM5114RS

4096-BIT (1024 x 4) CMOS STATIC RAM (E3-S-010-32)

GENERAL DESCRIPTION

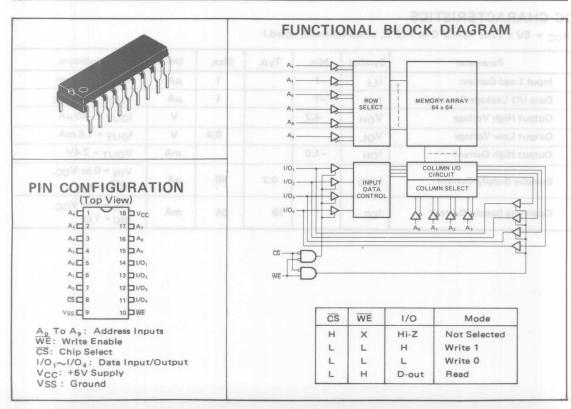
The Oki MSM5114 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable Silicon Gate CMOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Microwatt power dissipation typical of all CMOS is exhibited in all static states. Directly TTL compatible inputs, outputs and operation from a single +5V supply simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM5114 series is offered in an 18-pin plastic (RS suffix) package. The series is guaranteed for operation from 0° C to 70° C and over a 4V to 6V power supply range.

FEATURES

- Fully Static Operation
- Low Power Dissipation
 40μW Max. Standby Power
 192 mW/MHz Max. Operating
 Power
- Data Retention to V_{CC}=2V
- Single 4 ~ 6V Power Supply
- High Density 300-mil 18-Pin Package
- Common I/O Capability using Three-State Outputs
- Directly TTL/CMOS Compatible
- Silicon Gate CMOS Technology
- Interchangeable with Intel 2114L Devices

	5114-2	5114-3	5114
Max. Access Time (NS)	200	300	450
Max. Operating Power (MW/MHz)	192	192	192
Max. Standby Power (μW)	40	40	40



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	Vcc	-0.3 to 7.0	V	
Input Voltage	VIN	-0.3 to V _{CC} + 0.3	V	Respect to VSS
Data I/O Voltage	V _D	-0.3 to V _{CC} + 0.3	V	an ingawa
Storage Temperature	T _{stg}	-55 to 150	°C	

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Supply Voltage	Vcc	4	5	6	V	5V ± 20%
Devices	VIH	2.4	5	Vcc	V	Parasat to V
Input Signal Level	VIL	-0.3	0	0.8	V	Respect to VSS
Operating Temperature	Topr	0	0.4811	70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V \pm 10%; Ta = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Input Load Current	ILI	S -1	is.	1	μΑ	V _{IN} = 0 to V _{CC}
Data I/O Leakage Current	ILO	-1	6	1	μΑ	V _{I/O} = 0 to V _{CC}
Output High Voltage	VOH	4.2	K -		V	I _{OUT} = -40 μA
Output Low Voltage	VOL	4		0.4	V	I _{OUT} = 1.6 mA
Output High Current	ГОН	-1.0			mA	V _{OUT} = 2.4V
Standby Supply Current	Iccs		0.2	50	μА	V _{IN} = 0 or V _{CC} , V _{CS} = V _{CC}
Operating Supply Current	Icc		19	35	mA	V _{IN} = 0 or V _{CC} , t _{RC} = 1 μs

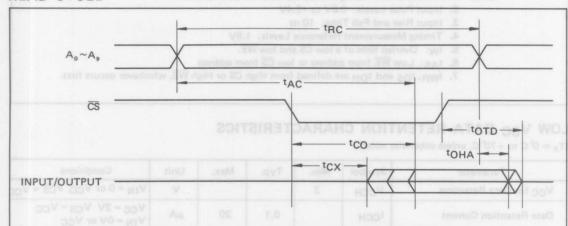
9

AC CHARACTERISTICS READ CYCLE

 $(V_{CC} = 5V \pm 10\%, T_a = 0^{\circ}C \text{ to } +70^{\circ}C)$

2	0	511	14-2	511	14-3	51	114	11-1-
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	tRC	200		300		450		ns
Access Time	tAC		200	/	300		450	ns
Chip Selection to Output Valid	tco	w	200		300		450	ns
Chip Selection to Output Active	tCX	20		20		20	3W	ns
Output 3-state from Deselection	tOTD		60		80		100	ns
Output Hold from Address Change	tOHA	10		10		10	TUTTUO	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{\text{CS}}$ and high $\overline{\text{WE}}$.

2. Input Pulse levels: 0.8V to +2.4V

3. Input Rise and Fail Time: 10 ns

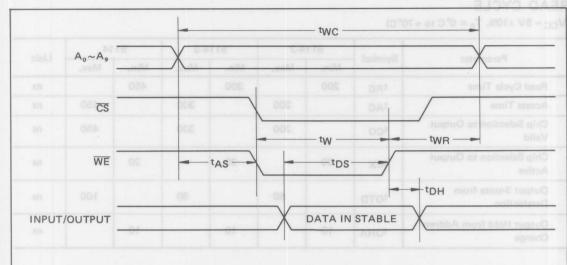
4. Timing Measurement Reference Levels: 1.5V
5. Output Load: 1 TTL Gate and C_L = 50 pF

WRITE CYCLE

 $(V_{CC} = 5V \pm 10\%, T_a = 0^{\circ}C \text{ to } +70^{\circ}C)$

D	C	511	14-2	511	14-3	51	14	Hair
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle Time	twc	200		300		450	HIV	ns
Write Time	tw	150		190		250	HOON	ns
Write Release Time	twR	20		30		50	5	ns
Address Setup Time	tAS	20		20		20	10.7	ns
Data Setup Time	tDS	120		150		200	сио	ns
Data Hold From Write Time	tDH	10		10		10		ns

WRITE CYCLE



Notes: 1. A Write occurs during the overlap of a low $\overline{\text{CS}}$ and low $\overline{\text{WE}}$.

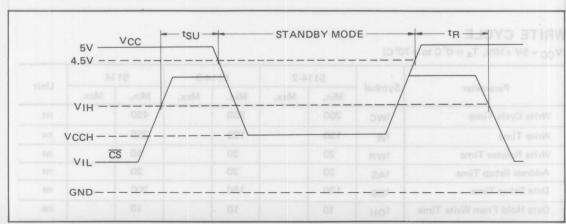
- 2. Input Pulse Levels: 0.8V to +2.4V
- 3. Input Rise and Fall Time: 10 ns
- 4. Timing Measurement Reference Levels: 1.5V
- 5. tw: Overlap time of a low CS and low WE.
- 6. tAS: Low WE from address or low CS from address
- 7. twR, tDS and tDH are defined from High CS or High WE, whichever occurs first.

LOW VCC DATA RETENTION CHARACTERISTICS

 $(T_a = 0^{\circ} C \text{ to } +70^{\circ} C, \text{ unless otherwise noted.})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
V _{CC} for Data Retention	VCCH	2			V	VIN = 0 or VCC, VCS = VCC
Data Retention Current	Іссн		0.1	20	μА	V _{CC} = 2V V _{CS} = V _{CC} V _{IN} = 0V or V _{CC}
CS to Data Retention Time	tsu	0	ing the dvi	nula enuncia	ns	l mania
Operation Recovery Time	tR	tRC	II :seniT	is 7 bins so	ns	0

LOW VCC DATA RETENTION WAVEFORM



CAPACITANCE

 $(T_a = 25^{\circ} C, f = 1 MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	C1/O			10	pF
Input Capacitance	CIN			8	pF

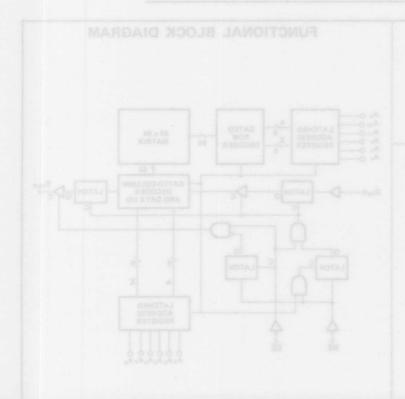
Note: This parameter is periodically sampled and not 100% tested.

0°C to 70°C and over a 4 V t

= High Density 300 mil 18-Pin Peckans

Registers

S3mW/MHz Max. Operating Powi Data Resention to Voc=2V Single 4 ~ 6V Power Supply







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MSM5104RS

4096-BIT (4096 x 1) CMOS STATIC RAM (E3-S-011-32)

GENERAL DESCRIPTION

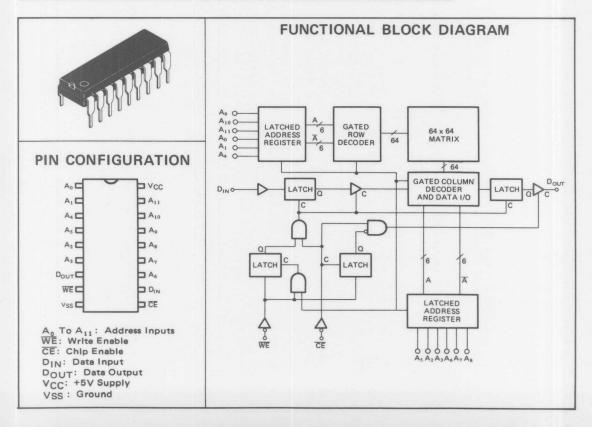
The Oki MSM5104 is a 4096-bit static Random Access Memory organized as 4096 words by 1 bit using Oki's reliable Silicon Gate CMOS technology. Microwatt power dissipation typical of all CMOS is exhibited in all static state. Directly TTL compatible inputs, output, operation from a single +5 V supply and on-chip address-data registers simplify system designs.

The MSM5104 series is offered in an 18-pin plastic (RS suffix) package. The series is guaranteed for operation from 0° C to 70° C and over a 4 V to 6 V power supply range.

FEATURES

- Low Power Dissipation
 40μW Max. Standby Power
 33mW/MHz Max. Operating Power
- Data Retention to V_{CC}=2V
- Single 4 ~ 6V Power Supply
- High Density 300-mil 18-Pin Package
- On-Chip Address and Data Registers
- Separate Data Input and Output
- Three-State Ouput
- Directly TTL/CMOS Compatible
- Silicon Gate CMOS Technology
- Pin-compatible with Mostek 4104,
 Interchangeable with Harris 6504

	5104-2	5104-3
Max. Access Time (NS)	200	300
Max. Operating Power (MW/MHz)	33	33
Max. Standby Power (μ)	40	40



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Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to 7.0	V
Input Voltage	VIN	-0.3 to V _{CC} + 0.3	V
Output Voltage	Vout	0 to V _{CC}	V
Storage Temperature	T _{stg}	-55 to 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Supply Voltage	Vcc	4	5	6	V	5V ± 20%	
	VIH	2.4	5	Vcc	V		
Input Signal Level	VIL	-0.3	0	0.8	V	Respect to VSS	
Operating Temperature	Topr	0		70	°C	0 1000	

DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%; Ta = 0^{\circ}C \text{ to } +70^{\circ}C, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Input Load Current	1 _{LI}	-1		1	μΑ	V _{IN} = 0 to V _{CC}
Output Leakage Current	ILO	-1		1	μА	V _{I/O} = 0 to V _{CC}
Output High Voltage	Voн	4.2			V	I _{OUT} = -40μA
Output Low Voltage	VOL			0.4	V	I _{OUT} = 1.6mA
Output High Current	ГОН	-1.0			mA	V _{OUT} = 2.4V
Standby Supply Current	Iccs		0.2	50	μΑ	VIN = 0 or VCC
Operating Supply Current	Icc			6	mA	V _{IN} = 0 or V _{CC} , t _{RC} = 1 μs

AC CHARACTERISTICS

 $(V_{CC}=5V\pm10\%, T_a=0^{\circ}C \text{ to } +70^{\circ})$

Parameter	Symbol	510	04-2	5104-3		
		Min.	Max.	Min.	Max.	Unit
Read/Write Cycle Time	tRC, tWC	300		420		ns
Chip Enable Access Time	tAC		200		300	ns
Chip Enable Pulse Width	tCE	200	_/888	300	AGRANA	ns
Chip Enable Off Time	tcc	100		120	наш	ns
Address Hold Time	tAH	40		50		ns
Address Setup Time	tAS	0		0		ns
Output Disable Time	tOFF	0	70	0	100	ns
Write Enable Pulse Width	tWP	100		130		ns
Write Enable Setup Time	tws	0		0		ns

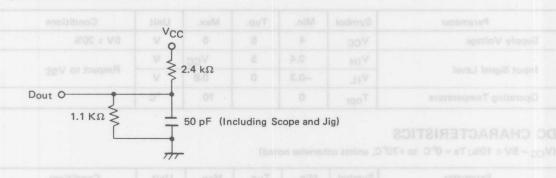
Parameter		5104-2		5104-3		UJUSS
	Symbol	Min.	Max.	Min.	Max.	Unit
Write Enable Hold Time	twH	120		150	needle V	ns
Data Setup Time	tDS	0		0	energie S.J.	ns
Data Hold Time	tDH	60		80		ns
Data Valid Time to Write Pulse	t _{DV}	0		0	againov n	ns
Write Enable Read Time	tWCL	150		200	Promptor Co.	ns

AC TEST CONDITIONS

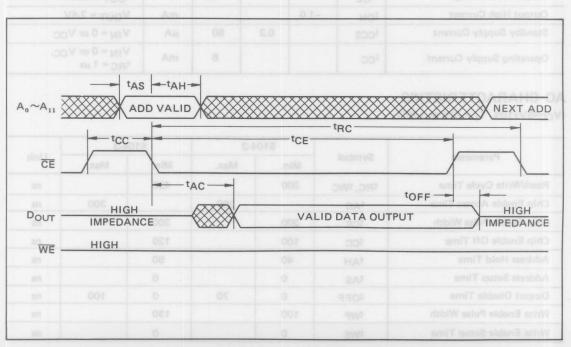
Input Pulse Levels: 0.8V to 2.4V

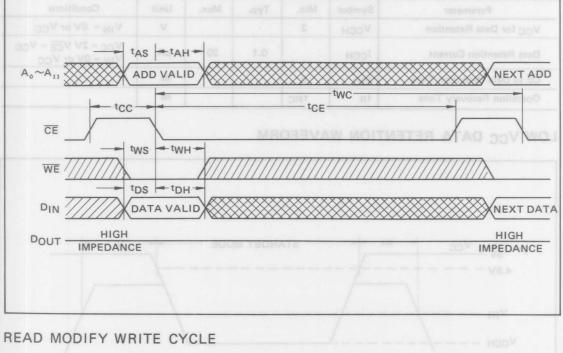
Timing Measurement Reference Levels: 1.5V

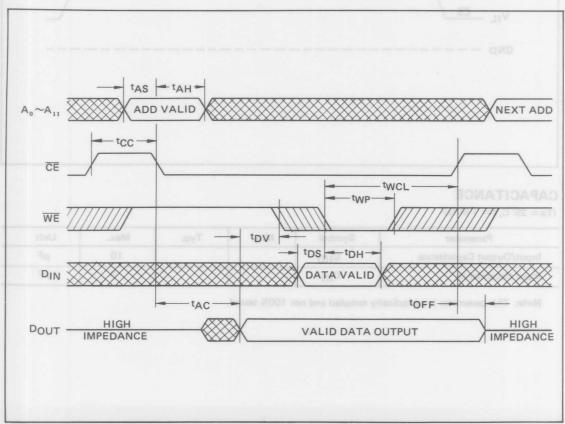
Input Rise and Fall Time: 10 ns



READ CYCLE





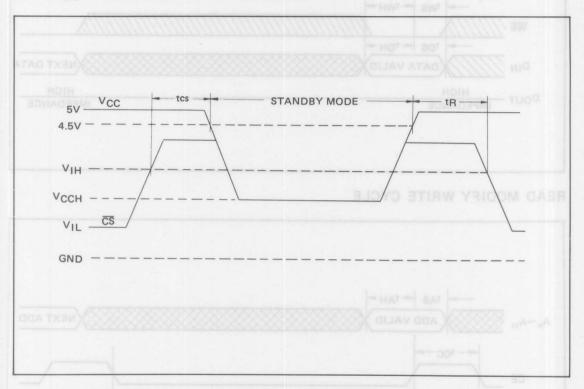


LOW VCC DATA RETENTION CHARACTERISTICS

 $(Ta = 0^{\circ} C \text{ to } +70^{\circ} C, \text{ unless otherwise noted.})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
V _{CC} for Data Retention	VCCH	2			V	VIN = 0V or VCC
Data Retention Current	Іссн		0.1	20	μА	V _{CC} = 2V V CE = V _{CC} V _{IN} = 0V or V _{CC}
CE to Data Retention Time	tsu	0			ns	11A~11A
Operation Recovery Time	tR	tRC			ns	

LOW VCC DATA RETENTION WAVEFORM



CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	C1/O			10	pF
Input Capacitance	CIN	000000000000000000000000000000000000000	XXXXXXX	8	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5115RS

4096-BIT (1024 x 4) CMOS STATIC RAM (E3-S-012-32)

GENERAL DESCRIPTION

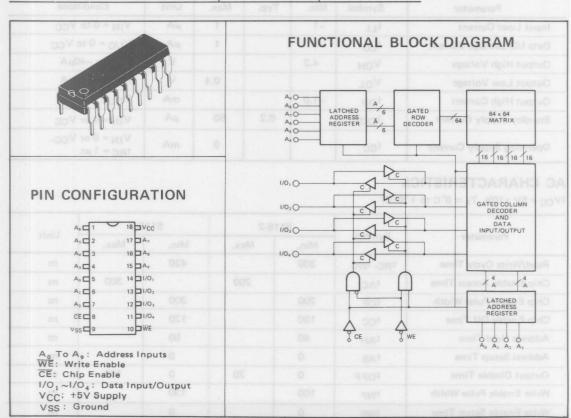
The Oki MSM5115 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable Silicon Gate CMOS technology. Microwatt power dissipation typical of all CMOS is exhibited in all static states. Directly TTL compatible inputs, outputs, operation from a single +5 V supply and on-chip address registers simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM5115 series is offered in an 18-pin plastic (RS suffix) package. The series is guaranteed for operation from 0° C to 70° C and over a 4 V to 6 V power supply range.

FEATURES

- Low Power Dissipation 40μW Max. Standby Power 33mW/MHz Max. Operating Power
- Data Retention to V_{CC} = 22V
- Single 4 ~ 6V Power Supply
- High Density 300-mil 18-Pin Package
- On-Chip Address Register
- Common I/O Capability using Three- State Outputs
- Directly TTL/CMOS Compatible
- Silicon Gate CMOS Technology
- Pin-compatible with Intel 2114,
 Interchangeable with Harris 6514

		5114-2	5115-3
	Max. Access Time (NS)	200	300
	Max. Operating Power (MW/MHz)	33	33
-	Max. Standby Power (μW)	40	40
	Max. Standby Power (μW)	40	40



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to 7.0	V
Input Voltage	VIN	-0.3 to V _{CC} + 0.3	V
Data I/O Voltage	VD	-0.3 to V _{CC} + 0.3	V
Storage Temperature	T _{stg}	-55 to 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Supply Voltage	Vcc	4	5	6	V	5V ± 20%
Input Signal Level	VIH	2.4	5	Vcc	V	SamWall's Max Operati
	VIL	-0.3	0	0.8	V	Respect to VSS
Operating Temperature	Topr	0	O STRIES	70	°C	Addres sevou no - s siduis

DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%; T_a = 0^{\circ}C \text{ to } +70^{\circ}C, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Input Load Current	ILI	-1		1	μΑ	V _{IN} = 0 to V _{CC}
Data I/O Leakage Current	ILO	-1		1	μΑ	V _{I/O} = 0 to V _{CC}
Output High Voltage	VOH	4.2			V	$I_{OUT} = -40\mu A$
Output Low Voltage	VOL			0.4	V	I _{OUT} = 1.6mA
Output High Current	ГОН	-1.0	A .		mA	V _{OUT} = 2.4V
Standby Supply Current	Iccs	1 3	0.2	50	μΑ	V _{IN} = 0 or V _{CC}
Operating Supply Current	Icc	- 0		6	mA	V _{IN} = 0 or V _{CC} , t _{RC} = 1 μs

AC CHARACTERISTICS

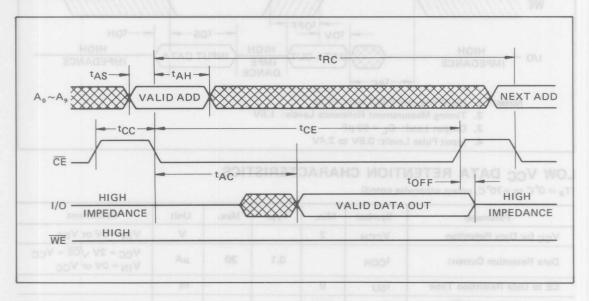
 $(V_{CC} = 5V \pm 10\%, T_a = 0^{\circ}C \text{ to } +70^{\circ}C)$

Downstan	Combal	51	15-2	51	15-3	
Parameter	Symbol	Min.	Max.	Min.	Max.	Unit
Read/Write Cycle Time	t _{RC} , t _{WC}	300		420	de 15	ns
Chip Enable Access Time	tAC		200		300	ns
Chip Enable Pulse Width	tCE	200		300		ns
Chip Enable Off Time	tcc	100		120	Gu sp	ns
Address Hold Time	tAH	40		50	100	ns
Address Setup Time	tAS	0		0	at emissa 1,	ns
Output Disable Time	tOFF	0	70	0	100	ns
Write Enable Pulse Width	tWP	100		130	V Supply	ns
Write Enable Setup Time	tws	0		0	bauos	ns

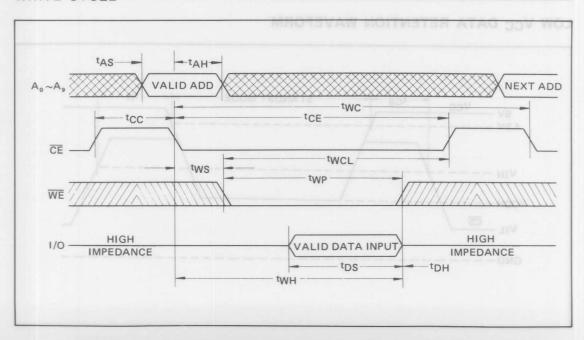
r		٦	
L	_	J	
	y	7	

Parameter	0 1 1	511	15-2	51	GOM GAB	
	Symbol	Min.	Max.	Min.	Max.	Unit
Write Enable Hold	twH	170		250	A1	ns
Data Setup Time	t _{DS}	100	8888888	130	1455555	ns
Data Hold Time	^t DH	0	500000	0	1/100000	ns
Data Valid Time to Write Pulse	tDV	0		0	00)	ns
Write Enable Read Time	tWCL	150		200		ns

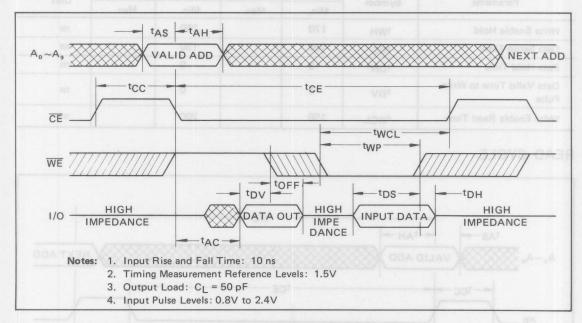
READ CYCLE



WRITE CYCLE



READ MODIFY WRITE CYCLE

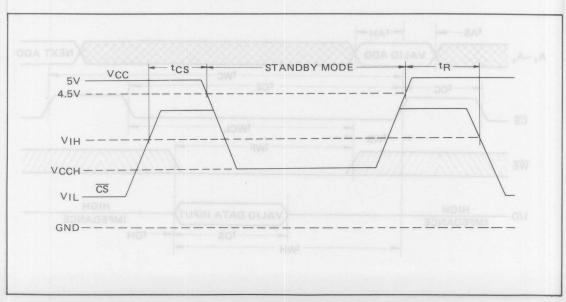


LOW VCC DATA RETENTION CHARACTERISTICS

 $(T_a = 0^{\circ} C \text{ to } +70^{\circ} C, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
V _{CC} for Data Retention	Vссн	2			V	V _{IN} = 0V or V _{CC}
Data Retention Current	Іссн		0.1	20	μА	$V_{CC} = 2V \sqrt{CE} = V_{CC}$ $V_{IN} = 0V \text{ or } V_{CC}$
CE to Data Retention Time	tsu	0			ns	
Operation Recovery Time	tR	tRC			ns	a joyo ario

LOW VCC DATA RETENTION WAVEFORM

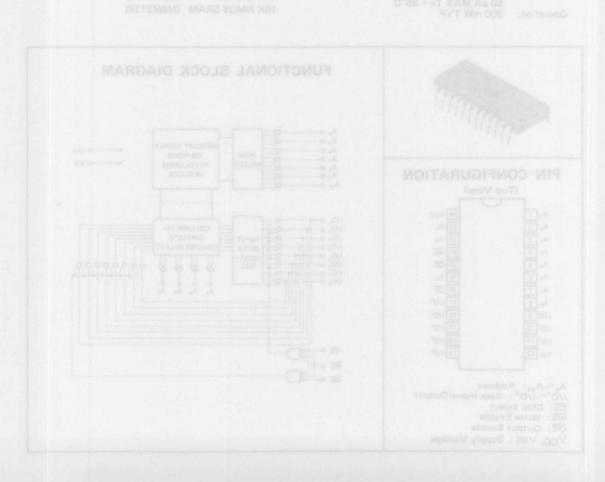


CAPACITANCE

 $(T_a = 25^{\circ} C, f = 1 MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	C _{1/O}			10	pF
Input Capacitance	CIN			8	pF

Note: This parameter is periodically sampled and not 100% tested.



MSM5128RS

2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-013-32)

GENERAL DESCRIPTION

MSM5128RS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5128RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50µA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, CS and $\overline{\text{OE}}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = -40°C to +85°C
- Low Power Dissipation
 - Standby;
- $1.0 \mu A MAX Ta = 25^{\circ} C$
- 10 μA MAX Ta = 60° C 50 μA MAX Ta = 85° C
- Operation; 200 mW TYP

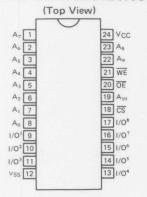
- High Speed (Equal Access and Cycle Time)
- MSM5128-12/15/20; 120 ns/150 ns/200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with

16K EPROM (MSM2716)

16K NMOS SRAM (MSM2128)



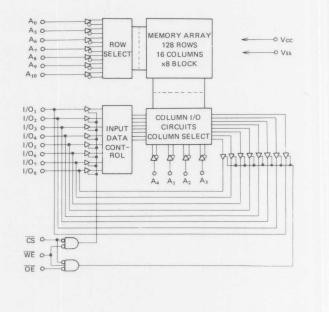
PIN CONFIGURATION



 $A_0 \sim A_{10}$: Address $I/O^1 \sim I/O^8$: Data Input/Output

CS: Chip Select WE: Write Enable OE: Output Enable VCC, VSS: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	CS	WE WE	OE S	I/O Operation
Standby	Hostel or	X xata	X	High Z
	L	Н	Н	High Z
Read	Au L	Н	L I-	Pour
Write	L	L	X	DIN

X: Hor L

ABSOLUTE MAXIMUM RATINGS

Rating	Rating Symbol		Unit	Conditions		
Supply Voltage	Vcc	-0.3 to 7.0	ro V	Barrant to CNID		
Input Voltage	VIN	-0.3 to V _{CC} + 0.3	V	Respect to GND		
Operating Temperature	Topr	-40 to 85	°C	D'all Inentui		
Storage Temperature	T _{stg}	-55 to 150	°C			
Power Dissipation	PD	1.0	W	1600		

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Supply Voltage	Vcc	4.5	5	5.5	V	5V ± 10%	
	VSS		0		V		
Data Storage Supply Voltage	VCCH	2	5	5.5	V	and the second	
Input Voltage	VIH	2.2		V _{CC} + 0.3	V	5V ± 10%	
Input voltage	VIL	-0.3		0.8	V		
Output Load	CL			100	pF	Outs	
Output Load	TTL			1			

DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%, T_a = -40^{\circ}C \text{ to } +85^{\circ}C)$

Param-	noi	Operat	MS	M5128	-12	MS	M5128	3-15	MS	M5128	3-20	11-14	т.	. 0 1'4'
eter	Syn	nbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Unit Test Condition	
Input Leakage Current		High 2	-1		1	-1		1	-1		1	μΑ	V _{IN} =	0 to V _{CC}
Output Leakage Current	I	LO	-1	41	11	-1		1	-1		1	μΑ	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = 0$ to V_{CC}	
	V	ОН	2.4			2.4			2.4			V	I _{OH} =	-1 mA
Output Voltage	V	OL			0.4			0.4	88	NIT!	0.4	V	IOL =	4 mA 28-12) 2.1 mA 28-15/20)
		Ta 25°C		0.1	1.0	0.7.0	0.1	1.0	0	0.1	1.0		- spe	Supply Volt
Standby Supply	Iccs	60° C		V	10) + aa	J to V	10		nY.	10	μΑ		V _{CC} - 0.2V 0 to V _{CC}
Current		85° C			50	38 a	-40	50	71	oT	50	. 971.0	VIN -	o to ACC
	IC	CS ₁		0.3	1	0 150	0.3	1		0.3	1	mA	CS = \	/IH Min. cycle
Oper- ating				40	60		37	55		35	50	mA	Min.	Ta = 0~85°C
Supply	C	CA		40	72		37	66		35	60		cycle	Ta=-40~85° C

AC CHARACTERISTICS

Test Condition

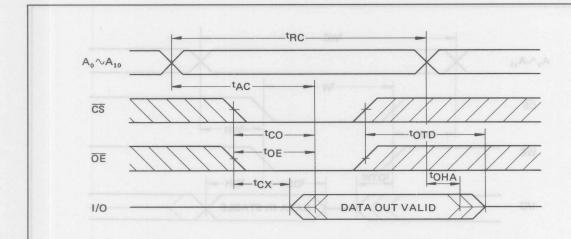
Parameter		Conditions
Input Pulse Level	0	V _{IH} =2.2V, V _{IL} =0.8V
Input Rise and Fall Times	0.0	10 ns
Input and Output Timing Reference Level	0.0-	1.5V
Output Load		C _L =100 pF, 1 TTL Gate

READ CYCLE

 $(V_{CC} = 5V \pm 10\%, T_a = -40^{\circ} C \text{ to } +85^{\circ} C)$

	0 1 1	MSM5128-12		MSM5128-15		MSM5128-20		Linit
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	tRC	120		150		200		ns
Address Access Time	tAC		120		150		200	ns
Chip Select Access Time	tco		120		150		200	ns
Output Enable to Output Valid	tOE		80		100		120	ns
Chip Selection to Output Active	tcx	10		15		20		ns
Output Hold Time From Address Change	tOHA	10		15		20		ns
Output 3-state from Deselection	tOTD	0	50	0	50	0	60	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{\text{CS}}$, a low $\overline{\text{OE}}$ and a high $\overline{\text{WE}}$.

2. tCX is specified from CS or OE, whichever occurs last.

3. totp is specified from $\overline{\text{CS}}$ or $\overline{\text{OE}}$, whichever occurs first.

4. toha and toto are specified by the time when DATA OUT is floating.

WRITE CYCLE

 $(V_{CC} = 5V \pm 10\%, T_a = -40^{\circ} C \text{ to } +85^{\circ} C)$

Parameter		MSM5128-12		MSM5128-15		MSM5128-20		Unit
	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle Time	twc	120		150		200		ns
Address to Write Setup Time	tAS	15		20		20	B SHE	ns
Write Time	tw	70		90		120		ns
Write Recovery Time	twR	15		20		20		ns
Data Setup Time	t _{DS}	50		60		80		ns
Data Hold from Write Time	tDH	5		10		10	33	ns
Output 3-State from Write	toTW		50		50		60	ns

Notes: 1. A Write Cycle occurs during the overlap of a low CS and a low WE.

2. OE may be both high and low in a Write Cycle.

3. t_{AS} is specified from \overline{CS} or \overline{WE} , whichever occurs last.

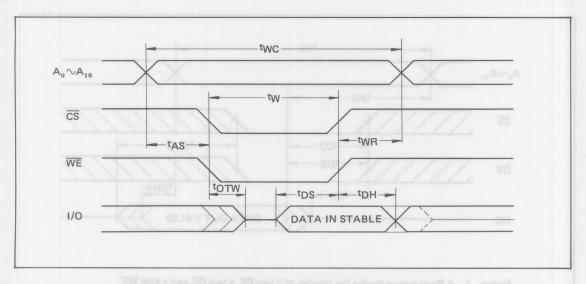
4. tw is an overlap time of a low CS and a low WE.

5. tWR, tDS and tDH are specified from CS or WE, whichever occurs first.

6. to Tw is specified by the time when DATA OUT is floating, not defined by output level.

7. When I/O pins are Data output mode, don't force inverse signal to those pins.

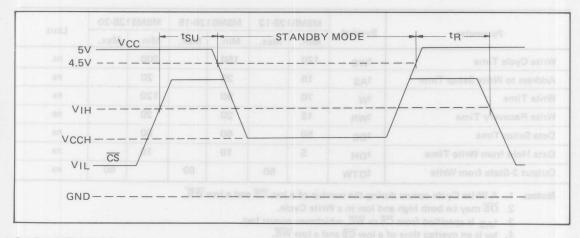
WRITE CYCLE



LOW VCC DATA RETENTION CHARACTERISTICS

 $(T_a = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions				
V _{CC} for Data Retention	VCCH	2			V	V _{IN} = 0V to V _{CC} , $\overline{\text{CS}}$ = V _{CC}				
Data Retention Current	Іссн		0.05	20	μΑ	V _{CC} = 2V \overline{CS} = V _{CC} V _{IN} = 0V to V _{CC}				
CS to Data Retention Time	tsu	0			ns	SIDVO STIRV				
Operation Recovery Time	tR	tRC			ns	072°08- = 47 307 4 V8 = V				



CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	C1/O			8	pF
Input Capacitance	c _{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5128-20GSK

2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-013-32)

GENERAL DESCRIPTION

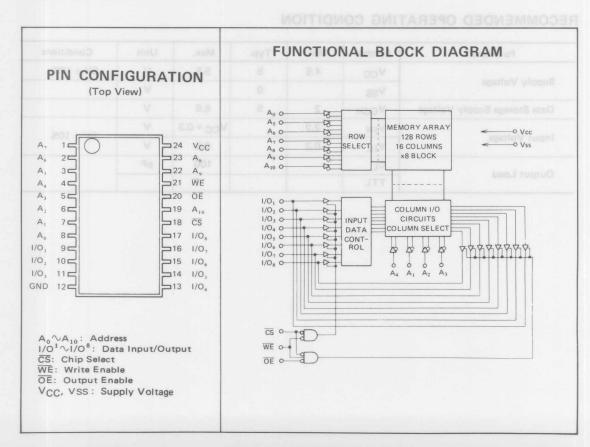
MSM5128GS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5128GS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50μ A) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, \overline{CS} and \overline{OE} signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = -40°C to +85°C
- Low Power Dissipation
 - Standby;
- 1.0 μ A MAX Ta = 25°C 10 μ A MAX Ta = 60°C
- $50 \,\mu\text{A} \,\text{MAX} \,\text{Ta} = 85^{\circ}\,\text{C}$
- Operation; 200 mW TYP

- High Speed (Equal Access and Cycle Time)
 MSM5128-20; 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 24 Pin Flat PKG



TRUTH TABLE

Mode	CS	WE	OE	I/O Operation
Standby	Н	×	×	High Z
	L	Н	Н	High Z
Read	L	Н	L	DOUT
Write	L	L	X	DIN

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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions	
Supply Voltage	Vcc	-0.3 to 7.0	V	D CALD	
Input Voltage	VIN	-0.3 to V _{CC} + 0.3	V	Respect to GND	
Operating Temperature	Topr	-40 to 85	°C	Single 5V Supply	
Storage Temperature	T _{stg}	-55 to 150	°C	Saltery Back-up at 2V	
Power Dissipation	PD	1.0	W	Low Power Dissipation	

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Supply Voltage	Vcc	4.5	5	5.5	V	5V ± 10%	
Supply Voltage	VSS		0		V	(Top)	
Data Storage Supply Voltage	VCCH	2	5	5.5	V		
Input Voltage	VIH	2.2	-CA	V _{CC} + 0.3	V	FM . 100/	
Input Voltage	VIL	-0.3	0 1A 0 1A	0.8	V	5V ± 10%	
Output Load	CL	8	io nA	100	pF	6	
Output Load	TTL			1		5	

DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%, T_a = -40^{\circ}C \text{ to } +85^{\circ}C)$

D			N	ISM5128-2	20			
Parameter	Syn	lode	Min. Typ. Max. Unit Tes		est Condition			
Input Leakage Current	J	1	-1		1	μΑ	V _{IN} = (to V _{CC}
Output Leakage Current	IL.	.0	-1		1	μΑ	$CS = V_{IH}$ or $OE = V_{IH}$ $V_{I/O} = 0$ to V_{CC} $I_{OH} = -1$ mA	
	Vo	ОН	2.4	-		V		
Output Voltage	V	OL			0.4	V		1 mA (5128-12) 2.1 mA (5128-15/20
		Ta 25°C	IO ATA	0.1	1.0			
Standby Supply	Iccs	60°C		-20	10	μΑ	$CS \ge V_{CC} - 0.2V$ $V_{IN} = 0$ to V_{CC}	
Current		85° C			50		VIN	210 466
	Ico	ICCS1		0.3	1	mA	CS = V t _{cyc} = I	IH Min. cycle
Operating	lo	0.4	el anuccio	35	50	mA	Min.	Ta = 0 ~ 85° C
Supply Current	10	ICCA		35	60	mA	cycle	$Ta = -40 \sim 85^{\circ} C$

AC CHARACTERISTICS

Test Condition

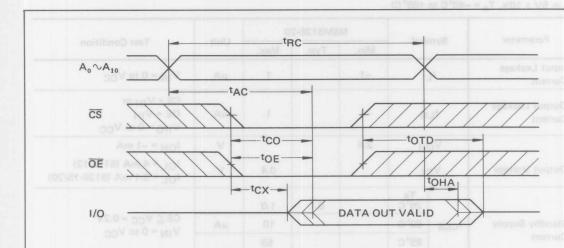
Parameter	Conditions		
Input Pulse Level	V _{IH} =2.2V, V _{IL} =0.8V		
Input Rise and Fall Times	10 ns		
Input and Output Timing Reference Level	1.5V		
Output Load	C _L =100 pF, 1 TTL Gate		

READ CYCLE

 $(V_{cc} = 5V \pm 10\%, T_a = -40^{\circ} C \text{ to } +85^{\circ} C)$

P00	Countries	MSM5	128-20	Unit	
Parameter	Symbol	Min.	Max.	Oni	
Read Cycle Time	^t RC	200	died ad vam	ns	
Address Access Time	†AC	W 10 23 mov	200	ns ns	
Chip Select Access Time	†CO	I was a to ami	200	ns	
Output Enable to Output Valid	tOE.	amis orby yd	120	ns	
Chip Selection to Output Active	tCX	20	ne zniq O\I ne	ns	
Output Hold Time from Address Change	toha	20		ns	
Output 3-state from Deselection	tOTD	0	60	ns	

READ CYCLE



- Notes: 1. A Read occurs during the overlap of a low $\overline{\text{CS}}$, a low $\overline{\text{OE}}$ and a high $\overline{\text{WE}}$.
 - 2. tCX is specified from CS or OE, whichever occurs last.
 - 3. toTD is specified from $\overline{\text{CS}}$ or $\overline{\text{OE}}$, whichever occurs first.
 - 4. toha and toto are specified by the time when DATA OUT is floating.

WRITE CYCLE

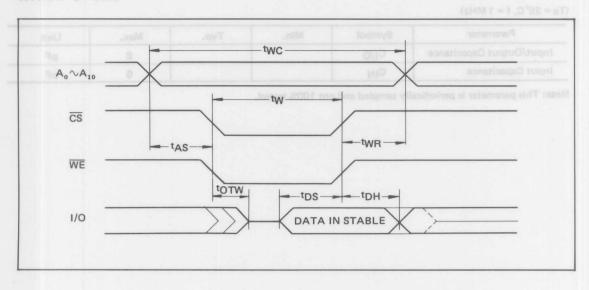
 $(V_{CC} = 5V \pm 10\%, T_a = -40^{\circ}C \text{ to } +85^{\circ}C)$

Parameter	Complete	MSM51	s foonl our	
Parameter	Symbol	Min.	Max.	Unit
Write Cycle Time	tWC	200	Load	ns ns
Address to Write Setup Time	†AS	20		ns
Write Time	tw	120		ns
Write Recovery Time	tWR	20		ns
Data Setup Time	^t DS	80	- C40°C to +81	ns
Data Hold from Write Time	^t DH	10		ns
Output 3-State from Write	toTW		60	ns

- Notes: 1. A Write Cycle occurs during the overlap of a low CS and a low WE.
 - 2. OE may be both high and low in a Write Cycle.
 - 3. tas is specified from CS or WE, whichever occurs last.

 - 4. tw is an overlap time of a low CS and a low WE.
 5. twn, tds and tdh are specified from CS or WE, whichever occurs first.
 - 6. to TW is specified by the time when DATA OUT is floating, not defined by output level.
 - 7. When I/O pins are Data output mode, don't force inverse signal to those pins.

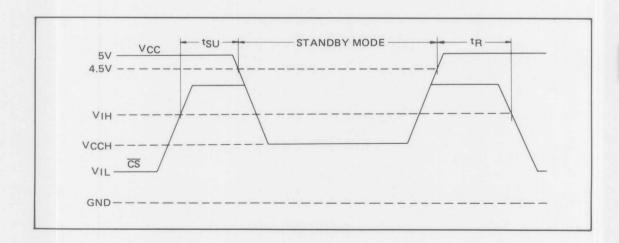
WRITE CYCLE



LOW VCC DATA RETENTION CHARACTERISTICS

 $(T_a = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
V _{CC} for Data Retention	Vссн	2			V	V _{IN} = 0V to V _{CC} , $\overline{\text{CS}}$ = V _{CC}
Data Retention Current	Іссн		0.05	20	μΑ	V _{CC} = 2V \overline{CS} = V _{CC} V _{IN} = 0V to V _{CC}
CS to Data Retention Time	tsu	0			ns	
Operation Recovery Time	tR	tRC			ns	

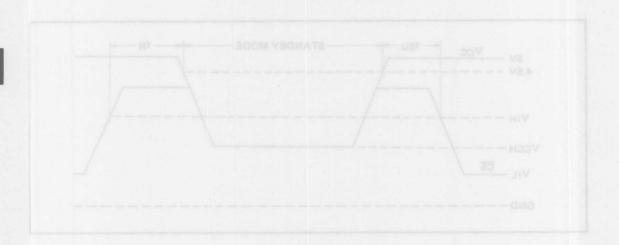


CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	CI/O			8	pF
Input Capacitance	CIN			6	A pF

Note: This parameter is periodically sampled and not 100% tested.



MSM5126RS

2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-014-32)

GENERAL DESCRIPTION

MSM5126RS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5126RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 30µA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, \overline{CS} and \overline{OE} signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = -30°C to +85°C
- Low Power Dissipation
 - Standby; $1.0 \mu A MAX T_a = 25^{\circ} C$
 - $5.0 \mu A MAX T_a = 60^{\circ} C$
 - 30 μ A MAX T_a = 85°C
 - Operation; 200 mW TYP

- High Speed (Equal Access and Cycle Time)
 MSM5126-20/25; 200 ns/250 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with

16K EPROM (MSM2716) 16K NMOS SRAM (MSM2128)

FUNCTIONAL BLOCK DIAGRAM

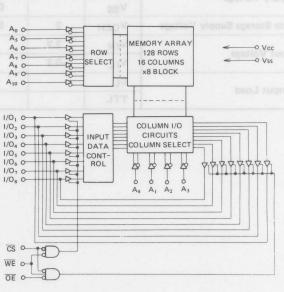
PIN CONFIGURATION (Top View)



 $A_0 \sim A_{10}$: Address $I/O^1 \sim I/O^8$: Data Input/Output

CS: Chip Select
WE: Write Enable
OE: Output Enable

VCC, VSS: Supply Voltage



TRUTH TABLE

Mode	CS	WE	ŌE	I/O Operation
Standby	Н	X	X	High Z
	L	Н	Н	High Z
Read	L	Н	L	Dout
Write	L	L	X	DIN

for incurs and outputs. And sinul To H .: X say is completely static, external clock and refreshing operations an

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions	
Supply Voltage	Vcc	-0.3 to 7.0	V	Respect to GND	
Input Voltage	VIN	-0.3 to V _{CC} + 0.3	V		
Operating Temperature	Topr	-30 to 85	°C	A Single 6V Supply	
Storage Temperature	T _{stg}	-55 to 150	°C	VS. 18 qui (1900) VS. 18 qui (
Power Dissipation	PD	1.0	W	Low Power Dissigntion	

RECOMMENDED OPERATING CONDITION

Parameter	CK DIAG	Symbol	Min.	Тур.	Max.	Unit	Conditions
Supply Voltage		Vcc	4.5	5	5.5	V	5V ± 10%
Supply Voltage	pply voltage			0		V	
Data Storage Supp	ly Voltage	Vссн	2	5	5.5	V	1/17
Input Voltage	DRY ARRAY	VIH	2.2	O A	V _{CC} + 0.3	V	
	58100700 58100700	VIL	-0.3	0 14	0.8	V	SUCCO MISS
		CL	100	O AA	100	pF	VacTi
Output Load		TTL			1		

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DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%, T_a = -30^{\circ}C \text{ to } +85^{\circ}C)$

				MS	/25	Unit	
Parameter	Symbol	Test Cond	lition	Min.	Тур.	Max.	Unit
Input Leakage Current	¹ LI	V _{IN} = 0 to V _{CC}	DA ¹	-1		1	μΑ
Output Leakage Current	ILO	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = 0$ to V_{CC}	- 001 -	-5		5	μΑ
Output	VOH	I _{OH} = -1 mA	1 //	2.4	///	20	V
Voltage	VOL	I _{OL} = 2.0 mA	X01			0.4	V
			Ta = 25°C		0.05	1.0	
Standby	Iccs	$\overline{\text{CS}} = \text{V}_{\text{CC}} - 0.5\text{V}$ $\text{V}_{\text{CC}} = 2\text{V} \sim 5.5\text{V}$	Ta = 60°C			5.0	μΑ
Supply		VCC = 2V ~ 5.5V	Ta = 85°C			30	
Current	ICCS ₁	$\overline{CS} = V_{IH}$ $t_{CYC} = Min. cycle$	enusco be	RA ¹ .r	3	mA	
Operating	1.	CS = OV, VIN = VIH/V	IL IOUT = 0 mA	e speciment	40	70	mA
Supply Current	ICCA	CS = OV, VIN = VCC/G	SND, IOUT = 0 mA	TO! bns /	30	55	mA

AC CHARACTERISTICS

Test Condition

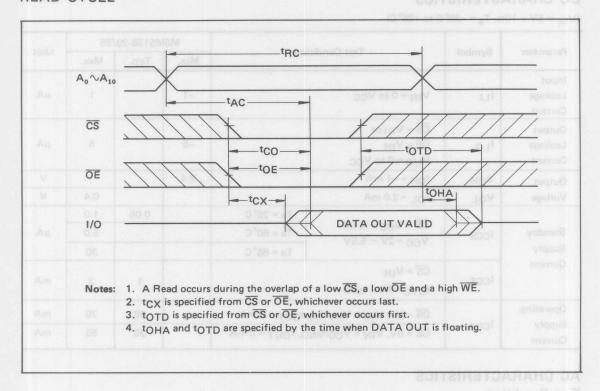
Parameter	Conditions
Input Pulse Level	V _{IH} = 2.4V, V _{IL} = 0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	2.2V 0.8V
Output Load	C _L =100 pF, 1 TTL Gate

READ CYCLE

 $(V_{CC} = 5V \pm 10\%, T_a = -30^{\circ} C \text{ to } +85^{\circ} C)$

120	Combal	MSM5126-2		MSM5	126-25	Unit
Parameter	Symbol	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	tRC	200	nt l	250	r 3-Stores for	ns
Address Access Time	tAC		200		250	ns
Chip Select Access Time	tco	to gallieve	200	Cycle occur	250	ns
Output Enable to Output Valid	tOE	a Wester Cyc	100	per porn mg	100	ns
Chip Selection to Output Active	tcx	10	of a low C	10	s ny is an	ns
Output Hold Time From Address Change	tOHA	10	the time w	10	S. LOTWIE	ns
Output 3-state from Deselection	tOTD	0	80	0	80	ns

READ CYCLE



WRITE CYCLE

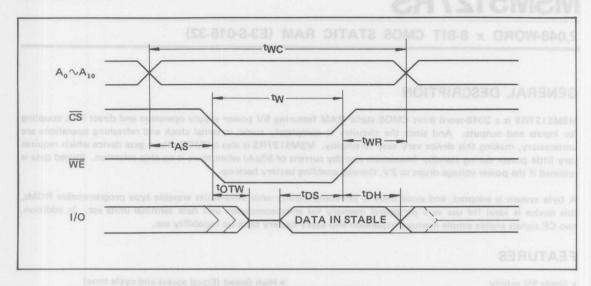
 $(V_{cc} = 5V \pm 10\%, T_a = -30^{\circ}C \text{ to } +85^{\circ}C)$

Parameter V8 0 V1 C	Course at	MSM5	126-20	MSM5	126-25	rugni Liuta
Parameter	Symbol	Min.	Max.	Min.	Max.	Unit
Write Cycle Time	twc	200		250	869,11	ns
Address to Write Setup Time	tAS	0		0		ns
Write Time	tW	160		200	- Table 1	ns
Write Recovery Time	tWR	10		10		ns
Data Setup Time	tDS	80	WS I	120	19790	ns
Data Hold from Write Time	^t DH	0		0		ns
Output 3-State from Write	toTW		80		80	ns

- Notes: 1. A Write Cycle occurs during the overlap of a low CS and a low WE.
 - 2. OE may be both high and low in a Write Cycle.
 - 3. tas is specified from CS or WE, whichever occurs last.
 - 4. tw is an overlap time of a low CS and a low WE.
 - 5. tWR, tDS and tDH are specified from CS or WE, whichever occurs first.
 - 6. to TW is specified by the time when DATA OUT is floating, not defined by output level.
 - 7. When I/O pins are Data output mode, don't force inverse signal to those pins.

9

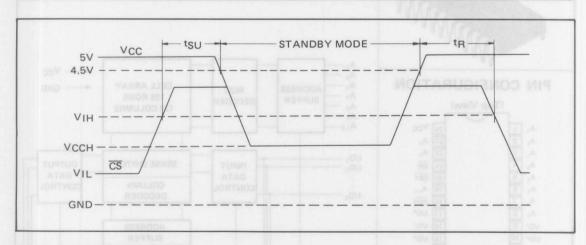
WRITE CYCLE



LOW VCC DATA RETENTION CHARACTERISTICS

 $(T_a = -30^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
V _{CC} for Data Retention	Vссн	2			V	V _{IN} = 0V to V _{CC}
Data Retention Current	Іссн		0.05	30	μА	$V_{CC} = 2V \sim 5.5V$ $V_{\overline{CS}} = V_{CC} - 0.5V$
CS to Data Retention Time	tsu	0			ns	
Operation Recovery Time	tR	tRC	FUN		ns	



CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	CI/O	Cle 1-3	5	10	pF
Input Capacitance	CIN		5	10	pF

Note: This parameter is periodically sampled and not 100% tested.

MSM5127RS

2,048-WORD x 8-BIT CMOS STATIC RAM (E3-S-015-32)

GENERAL DESCRIPTION

MSM5127RS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5127RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50μ A) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, two CE signals enable simple memory expansion and easily battery back-up capability etc.

FEATURES

- Single 5V supply
- Battery back-up at 2V
- Low power dissipation

Standby; $1.0 \mu A MAX Ta = 25^{\circ} C$

 $10 \,\mu\text{A} \,\text{MAX} \,\text{Ta} = 60^{\circ}\,\text{C}$

50 μA MAX Ta = 85°C

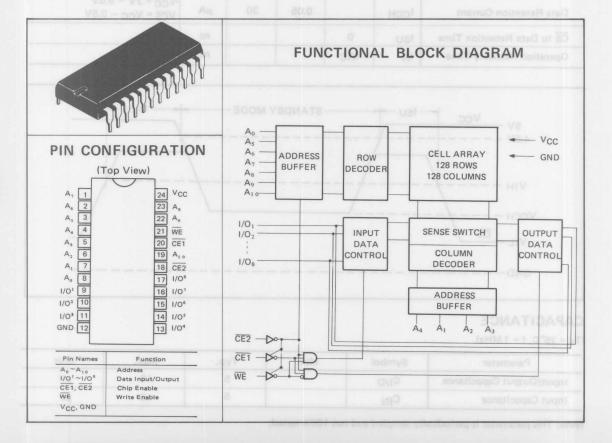
Operation; 200 mW TYP

High Speed (Equal access and cycle time)
 MSM5127-15/20: 150 ns/200 ns MAX

- Direct TTL compatible (Input and Output)
- 3-State output
- Pin compatible with

16 K EPROM (MSM2716)

16 K NMOS SRAM (MSM2128)



TRUTH TABLE

Mode	CE1	CE2	WE	I/O Operation
Standby	X X	Н	×	High Z
Dand	H	NAT COM NEW	×	High Z
Read	gV Au L 1	L T	H I-	DOUT
Wire	L	L	L	D _{IN}

X: H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Onit	Note
Supply Voltage	VCC	-0.3 ~ 7.0	V	Respect
Input Voltage	VIN	-0.3 ~ V _{CC} + 0.3	V	to GND
Operating Temperature	Ta	− 40 ~ 85	°C	Iperating -
Storage Temperature	T _{stg}	− 55 ~ 150	°C	The state of the s
Power Dissipation	Pd	1.0	W	

RECOMMENDED OPERTING CONDITION

Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
Cupply Voltage	Vcc	4.5	5	5.5	V	5V ±10%
Supply Voltage	GND		0	lava 1	V	aniT
Data Storage Supply Voltage	VCCH	2	5	5.5	V	uO.
Input Voltage	VIH	2.2		V _{CC} +0.3	V	5V ±10%
Input Voltage	VIL	-0.3		0.8	V	30 110%
Output Load	CL			100	pF	AD CAL
	TTL		- 1	1 0 0		OFEVE PO

DC CHARACTERISTICS

(VCC = 5V ± 10% Ta = -40 ~ 85°C

2	0		MS	M5127	7-15	MS	M5127	7-20	I Inia		Test Condition
Parameter	Sym	lodi	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit		lest Condition
Input Leakage Current	0 t ₁	ILI			1	-1	1	μΑ	V _{IN} =	0 to V _{CC}	
Output Leakage Current	ILO		-1		1	-1		1	μΑ		V _{IH} or CE1 = V _{IH} = 0 to V _{CC}
O	Vo	ЭН	2.4			2.4			V	I _{OH} =	-1 mA
Output Voltage	V	OL			0.4			0.4	V	I _{OL} = 2.1 mA	
		Ta 25°C		0.1	1.0		0.1	1.0	A CO B		ZAM TEU INSS
Standby Supply	Iccs	60°C			10		- 49	10	μΑ		V _{CC} - 0.2V 0 to V _{CC}
Current	tink	85°C		911	50			50	2	VIIN	Rating
	Ico	CS ₁		0.3	1		0.3	1	mA	CE2 = V _{IH} t _{cyc} = min cycle	
Operating	- 0			37	55		35	50	mA	Min.	Ta = 0 ~ 85° C
Supply Current	IC	CA		37	66		35	60	mA	cycle	Ta = -40 ~ 85° C

AC CHARACTERISTICS

TEST CONDITION

Parameter	Conditions
Input Pulse Level	V _{IH} = 2.2V, V _{IL} = 0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C _L = 100 pF, 1 TTL Gate

READ CYCLE

 $(V_{CC} = 5V \pm 10\%, Ta = -40 \sim 85^{\circ}C)$

	0 1 1	MSM5127-15		MSM5	Unit	
Parameter	Symbol	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	tRC	150		200		ns
Address Access Time	tAC		150		200	ns
CE2 Access Time	tCO2		150		200	ns
CE1 Access Time	tCO1		100		120	ns
Chip Selection to Output Active	tcx	15		20		ns
Output Hold Time From Address Change	tOHA	15		20		ns
Output 3-state from Deselection	tOTD	0	50	0	60	ns

NOTES: 1. A read occurs during the overlap of a low $\overline{\text{CE2}}$, a low $\overline{\text{CE1}}$ and a high $\overline{\text{WE}}$.

2. t_{CX} is specified from $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$, whichever occurs last.

3. tOTD is specified from CE1 or CE2, whichever occurs first.

4. toha and toto are specified by the time when DATA OUT is floating.

WRITE CYCLE

 $(V_{CC} = 5V \pm 10\%, Ta = -40 \sim 85^{\circ}C)$

Parameter		lytax.	Typ	MSM	5127-15	MSM	5127-20	I Imia
	v		Symbol	Min.	Max.	Min.	Max.	Unit
Write Cycle Time			tWC	150		200		ns
Address to Write Setup Time	Aq	20	tAS	20	Гесы	20	tention Cur	ns
Write Time			tw	90	Lund	120	etented ete	ns
Write Recovery Time	265		tWR	20	20 S	20	n Recover	ns
Data Setup Time		Jan Ser	tDS	60	- "	80		ns
Data Hold from Write Time			^t DH	10		10		ns
Output 3-State from Write			tOTW		50		60	ns

NOTES: 1. A Write Cycle occurs during the overlap of a low $\overline{\text{CE1}}$, a low $\overline{\text{CE2}}$ and a low $\overline{\text{WE}}$.

2. tas is specified from CE1 or CE2 or WE, whichever occurs last.

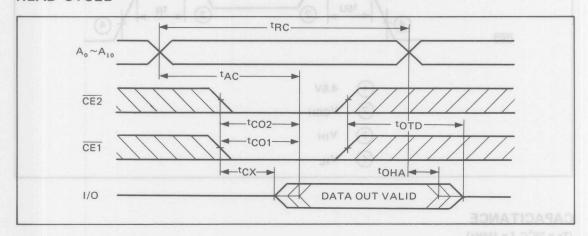
3. tw is an overlap time of a low CE1, a low CE2 and a low WE.

4. tWR, tDS and tDH are specified from CE1 or CE2 or WE, whichever occurs first.

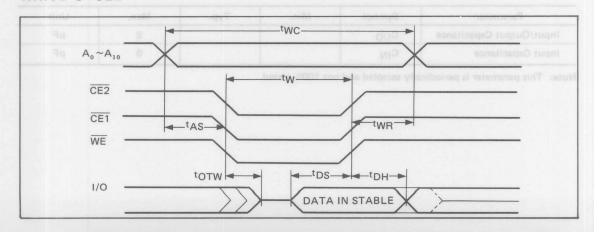
5. to TW is specified by the time when DATA OUT is floating, not defined by output level.

6. When I/O pins are Data output mode, don't force inverse signal to those pins.

READ CYCLE



WRITE CYCLE

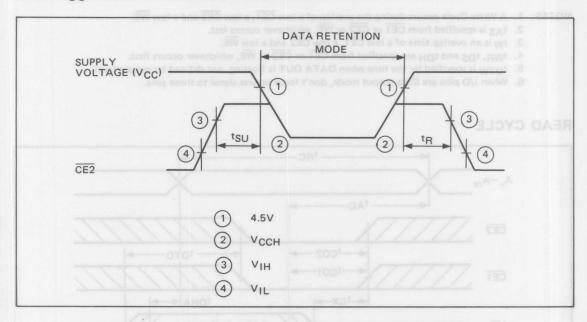


LOW VCC DATA RETENTION CHARACTERISTICS

(Ta = -40 to $+85^{\circ}$ C, unless otherwise noted)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
V _{CC} for Data Retention	Vссн	2	DOM: YO		V	$\frac{V_{IN}}{CE2} = 0V \text{ to } V_{CC}$
Data Retention Current	ССН	20	0.05	20	μΑ	$Vcc = 2V, \overline{CE2} = Vcc$ $V_{IN} = 0V \text{ to } Vcc$
CE to Data Retention Time	tsU	0	Ma		ns	9/m11, 91
Operation Recovery Time	tR	tRC	RW ²		ns	simil yracovart an

LOW VCC DATA RETENSION WAVEFORM



CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	C _{I/O}	- OWI		8	pF
Input Capacitance	CIN			6	A pF

Note: This parameter is periodically sampled and not 100% tested.

MSM5129RS

2.048-WORD x 8-BIT CMOS STATIC RAM (E3-S-016-32)

GENERAL DESCRIPTION

MSM5129RS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5129RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50µA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, two CE signals enable simple memory expansion and easily battery back-up capability etc.

FEATURES

- Single 5V supply
- Battery back-up at 2V
- Low power dissipation

Standby; $1.0 \mu A MAX Ta = 25^{\circ} C$

10 μA MAX Ta = 60° C

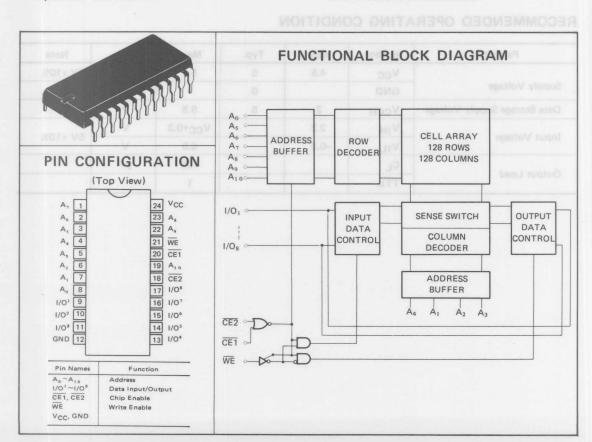
 $50 \mu A MAX Ta = 85^{\circ} C$

Operation: 200 mW TYP

- High Speed (Equal access and cycle time)
 MSM5129-15/20: 150 ns/200 ns MAX
- Direct TTL compatible (Input and Output)
- 3-State output
- Pin compatible with

16 K EPROM (MSM2716)

16 K NMOS SRAM (MSM2128)



TRUTH TABLE

Mode	CE1	CE2	WE	I/O Operation
STANDBY	Н	×	×	High Z
STANDBY	L	Н	×	riigii Z
READ	L	L	Н	DOUT
WRITE	L	L	L	DIN

Hor L' X CAMOS static RAM featuring BV power supply operation and direct TTL coupling L' Hor L' CAMOS are since the circultry is completely static, external clock and refreshing operations are

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value Value	Unit	Note
Supply Voltage	Vcc	− 0.3 ~ 7.0	V	Respect
Input Voltage	VIN	-0.3 ~ V _{CC} + 0.3	V	to GND
Operating Temperature	Ta bosos Apill	-40 ~ 85	°C	sque V8 vienià
Storage Temperature	T _{stg}	− 55 ~ 150	°C	Bartisty back-u
Power Dissipation	Pd	1.0	W	BIO TENEDO IS DO

RECOMMENDED OPERATING CONDITION

Parame	eter	Symbol	Min.	Тур.	Max.	Unit	Note
Supply Voltage		Vcc	4.5	5	5.5	٧	5V ±10%
		GND		0	a result	V	
Data Storage Su	ipply Voltage	VCCH	2	5	5.5	V	
Innut Valtage	YARRA LIEG	VIH	2.2	- A	V _{CC} +0.3	V	EV - 100
128 ROWS		VIL	-0.3	A	0.8	V	5V ±10%
Output Lood	138 COLUMNS	CL			100	PF M	PIN CC
Output Load		TTL		Ag grand	1	(welV-goT)	

DC CHARACTERISTICS dead a base 150 well a 350 well a to getteve entire provide tuposo base A .1 2510 M

 $(V_{CC} = 5V \pm 100\% Ta = -40 \sim 85^{\circ}C)$

D	Complete	MS	SM5129-	15	MS	SM5129	-20	Linie	-	0
Parameter	Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit		est Condition
Input Leakage Current	ILI	-1		1	-1		1	μΑ	V _{IN} =	0 to V _{CC}
Output Leakage Current	ILO	-1 81	SMS 129	1	-1 lockmy		1	μА		V _{IH} or CE1 =V _{IH} =0 to V _{CC}
XEN	Vон	2.4			2.4			V	IOH=	–1 mA
Output Voltage	VOL		0	0.4	DW 2A		0.4	V	I _{OL} =	2.1 mA
100 201	Ta 25°C		0.1	1.0	VI	0.1	1.0			Vcc-0.2V Vcc-0.2V or ≦0.2V
				10	20		10		V _{IN} =	0 to Vcc
Standby Supply	ICCS 60°C			10			10	μΑ	CE1≥	Vcc-0.2V
Current	85° C			50	WTO		50	-		Vcc–0.2V or ≤ 0.2 V ot Vcc
	Iccs1	and a fo	0.6	2	wal s to	0.6	2	mA	CE= \	/IH min cycle
Operating			37	55	N CE2 at	35	50	mA	Min.	Ta=0~85°C
Supply Current	ICCA	usas 18v	37	66	ID to FB	35	60	mA	cycle	Ta=-40~85°C

AC CHARACTERISTICS

TEST CONDITION

Parameter	Conditions			
Input Pulse Level	V _{IH} = 2.2V, V _{IL} = 0.8V			
nput Rise and Fall Times	10 ns			
nput and Output Fiming Reference Level	1.5V			
Output Load	C _L = 100 pF, 1 TTL Gate			

READ CYCLE

 $(V_{CC} = 5V \pm 10\%, Ta = -40 \sim 85^{\circ}C)$

Parameter	Symbol	MSM5129-15		MSM5129-20		Unit
Parameter	Symbol	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	tRC	150		200		ns
Address Access Time	tAC		150		200	ns
CE1 Access Time	tCO1		150	135	200	ns
CE2 Access Time	tCO2	1	150	195	200	ns
Chip Selection to Output Active	tCX	15		20		ns
Output Hold Time from Address Change	tOHA	15		20		ns
Output 3-state from Deselection	tOTD	0	50	0	60	ns

NOTES: 1. A read occurs during the overlap of a low CE2, a low CE1 and a high WE.

- 2. tCX is specified from CE1 or CE2, whichever occurs last.
- 3. toTD is specified from CE1 or CE2, whichever occurs first.
- 4. toha and toto are specified by the time when DATA OUT is floating.

WRITE CYCLE

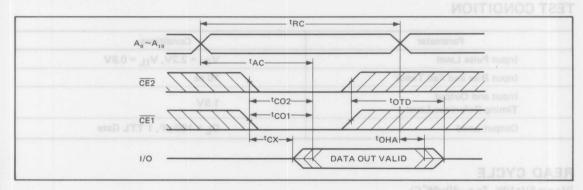
 $(V_{CC} = 5V \pm 10\%, Ta = -40 \sim 85^{\circ}C)$

HIA CEZ =VIJH OF CET=VIJH			MSM5129-15		MSM5129-20		Unit
Parameter		Symbol	Min.	Max.	Min.	Max.	Unit
Write Cycle Time		tWC	150		200	eges	ns
Address to Write Setup Time		tAS	20		20		ns
Write Time	0.1	tw	90	0	120		ns
Write Recovery Time		tWR	20		20		ns
Data Setup Time	10	tDS	60		80	und	ns
Data Hold from Write Time		tDH	10		10	ylgo	ns
Output 3-State from Write	50	toTW	08	50	85°C	60	ns

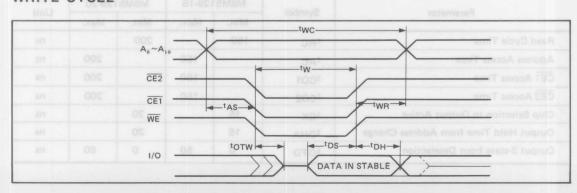
NOTES: 1. A Write Cycle occurs during the overlap of a low $\overline{\text{CE1}}$, a low $\overline{\text{CE2}}$ and a low $\overline{\text{WE}}$.

- 2. tas is specified from CE1 or CE2 or WE, whichever occurs last.
- 3. tw is an overlap time of a low CE1, a low CE2 and a low WE.
- 4. tWR, tDS and tDH are specified from CE1 or CE2 or WE, whichever occurs first.
- 5. toTW is specified by the time when DATA OUT is floating, not defined by output level.
- 6. When I/O pins are Data output mode, don't force inverse signal to those pins.

READ CYCLE



WRITE CYCLE



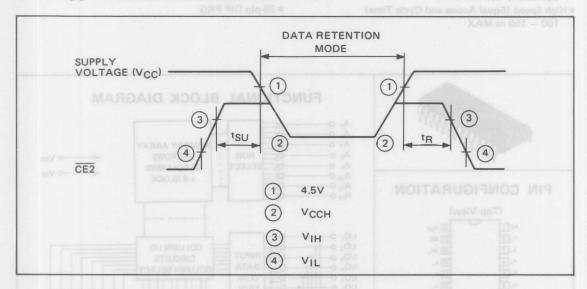
9

LOW VCC DATA RETENTION CHARACTERISTICS

 $(Ta = -40 \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
V _{CC} for Data Retention	1					$ \overline{CE2} = Vcc $ $ \overline{CE1} = 0 \text{ or } Vcc $ $ V_{1N} = 0 \text{ to } Vcc $ $ \overline{CE1} = Vcc $ $ \overline{CE2} = 0 \text{ or } Vcc $ $ V_{1N} = 0 \text{ to } Vcc $
ilicon gate davice which requires tion, isable type programmable ROMs, minet units a.e., its skillens, RE	e-violet er	od a glad there is no with ults	mpatibility	went of the colors of the colo	ninge there	$\frac{\text{Vcc} = 2\text{V, }\overline{\text{CE2}} = \text{Vcc}}{\overline{\text{CE1}} = 0 \text{ or } \text{Vcc}}$ $\frac{\text{Vin} = 0 \text{ to } \text{Vcc}}{\text{Vin}} = 0 \text{ to } \text{Vcc}$
Data Retention Current	Іссн	s of other	0.05	20	μΑ	Vcc = 2V, CE1 = Vcc CE2 = 0 or Vcc V _{IN} = 0 to Vcc
CE to Data Retention Time	tsU	0			ns	EATURES
Operation Recovery Time	t _R	tRC	1 -		ns	ulamiQ VP shei2

LOW VCC DATA RETENSION WAVEFORM



CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	C _{1/O}			8	pF
Input Capacitance	CIN		o ,30	6	pF

Note: This parameter is periodically sampled and not 100% tested.

MSM5165RS

8,192-WORD x 8-BIT CMOS STATIC RAM (E3-S-017-32)

GENERAL DESCRIPTION

MSM5165 is a 8192 word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5165 is also a CMOS silicon gate device which requires very low power during standby (standby current of 1mA) when there is no chip selection.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, \overline{CE}_1 CE $_2$ and \overline{OE} signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

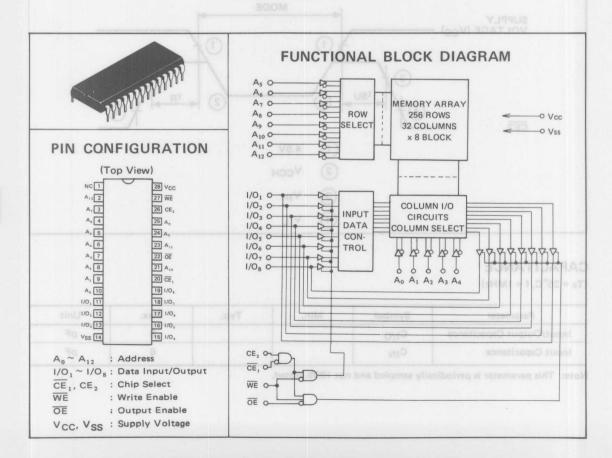
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
 - Standby; 5.5 mW MAX Operation; 495 mW MAX
- High Speed (Equal Access and Cycle Time)

100 - 150 ns MAX

- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with

64K EPROM (MSM2764) 64K NMOS SRAM (MSM2188)

• 28-pin DIP PKG



TRUTH TABLE

Mode	CE,	CE ₂	WE	ŌĒ	I/O Operation	
notibe	H est Co	X sinU	MU X X		High Z	
Standby	X	L	X	×	High Z	
	L	Н	Н	Н	High Z	
Read	L	Н	Н	L	DOUT	
Wreite	30 L aiv =	35 H	L	×	DIN	

X:HorL

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions	
Supply Voltage	Vcc	C -0.3 to 7.0		Barrant to CND	
Input Voltage	VIN	-0.5 to V _{CC} + 0.5	V	Respect to GND	
Operating Temperature	Topr	0 to 70	°C	700	
Storage Temperature	T _{stg}	-55 to 150	°C	106	
Power Dissipation	PD	1.0	W	18001	

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Supply Voltage	Vcc	4.5	5	5.5	V	5V ± 10%
	VSS		0		V	
Data Storage Supply Voltage	Vссн	2	5	5.5	V	- Judiii
Input Voltage	VIH	2.2		V _{CC} + 0.5	V	5V ± 10%
	VIL	-0.3		0.8	V	
Output Load	CL			100	pF	Output
	TTL			1		

DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%, T_a = 0^{\circ}C \text{ to } +70^{\circ}C)$

Paramter	Symbol		MSM5165	5	Unit	Test Condition
Paramter	Symbol	Min.	Тур.	Max.	Unit	lest Condition
Input Leakage Current	I _{LI}	-1		H 1	μΑ	V _{IN} = 0 to V _{CC}
Output Leakage Current	I _{LO} TO H	× -1		1	μА	$\overline{CE}_1 = V_{IH} \text{ or } CE_2 = V_{IL} \text{ or }$ $\overline{OE} = V_{IH}$ $V_{I/O} = 0 \text{ to } V_{CC}$
Output	VOH	2.4			V	I _{OH} = -1 mA
Voltage	VOL			0.4	V	I _{OL} = 2.1 mA
anditions set to GND		lnti V	7.0	oteV to E.O.	mA	$\overline{CE}_1 \stackrel{>}{=} V_{CC} - 0.2V$, $CE_2 \stackrel{>}{=} V_{CC} - 0.2V$ or $CE_2 \stackrel{\leq}{=} 0.2V$ $V_{IN} = 0$ to V_{CC}
Standby Supply		o°.		0.5 to V _C		$CE_2 \le 0.2V$ $V_{IN} = 0 \text{ to } V_{CC}$
Current	I _{CCS1}	W	001	3	mA	$\overline{CE}_1 = V_{IH}, CE_2 = V_{IL}$ $t_{Cyc} = Min, cycle$
Operating Supply Current	ICCA			90	mA mA	Min. cycle $T_a = 0 \sim 70^{\circ} C$

AC CHARACTERISTICS

Test Condition

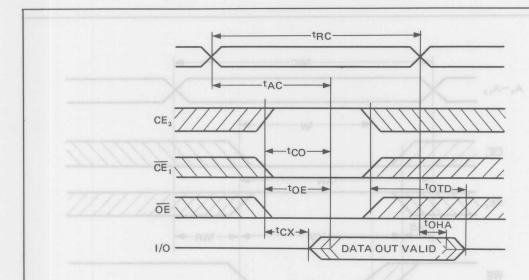
Parameter		Conditions
Input Pulse Level		V _{IH} =2.2V, V _{IL} =0.8V
Input Rise and Fall Times	0.0	10 ns
Input and Output Timing Reference Level	-0.3	1.5V
Output Load		C _L =100 pF, 1 TTL Gate

READ CYCLE

 $(V_{CC} = 5V \pm 10\%, T_a = 0^{\circ}C \text{ to } 70^{\circ}C)$

	0	MSM5165-10		MSM5165-12		MSM5165-15		11-24
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	150 150 100	Unit
Read Cycle Time	tRC	100		120		150		ns
Address Access Time	tAC		100		120		150	ns
Chip Enable Access Time	tco		100	-	120		150	ns
Output Enable to Output Valid	tOE		60		80		100	ns
Chip Selection to Output Active	tcx	10		10		15		ns
Output Hold Time From Address Change	tOHA	10		10		15		ns
Output 3-state from Deselection	tOTD	0	40	0	50	0	50	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low \overline{CE}_1 , a high CE_2 , a low \overline{OE} and a high \overline{WE} .

2. t_{CX} is specified from \overline{CE}_1 , CE_2 or \overline{OE} , whichever occurs last.

3. t_{OTD} is specified from \overline{CE}_1 , CE_2 or \overline{OE} , whichever occurs first.

4. toha and toto are specified by the time when DATA OUT is floating.

WRITE CYCLE

 $(V_{cc} = 5V \pm 10\%, T_a = 0^{\circ}C \text{ to } +70^{\circ}C)$

Item	Combal	MSM5165-10		MSM5165-12		MSM5165-15		I India
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle Time	twc	100		120		150		ns
Address to Write Setup Time	tAS	0	DARA	0	CHTHE	0	ATAG	ns
Write Time	tw	60		70	aton salw	90	0°C, unle	+ of Ons
Write Recovery Time	tWR	15		15		20		ns
Data Setup Time	tDS	40	HAKI	50		60	101	ns
Data Hold from Write Time	^t DH	0		0		0		ns
Output 3-State from Write	toTW	0	40	0	50	0	50	ns
Chip Selection to End of Write	tCW	80		90		110		ns
Address Valid to End of Write	t _{AW}	80		90		110		ns
Output Active from End of Write	twx	5		5	Hool	10	Current	ns

Note: 1. A Write Cycle occurs during the overlap of a low \overline{CE}_1 , a high CE_2 and a low \overline{WE} .

2. OE may be both high and low in a Write Cycle.

3. t_{AS} is specified from \overline{CE}_1 , CE_2 or \overline{WE} , whichever occurs last.

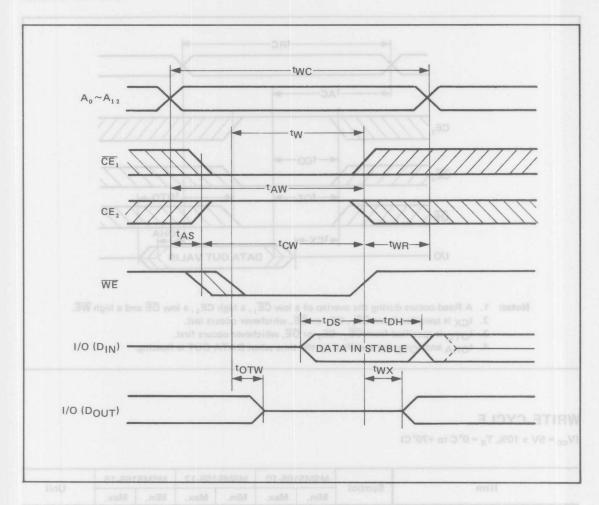
4. t_W is an overlap time of a low \overline{CE}_1 , a high CE_2 and a low \overline{WE} .

5. twR, tDS and tDH are specified from $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$ or $\overline{\text{WE}}$, whichever occurs first.

6. to Tw is specified by the time when DATA OUT is floating, not defined by output level.

7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE

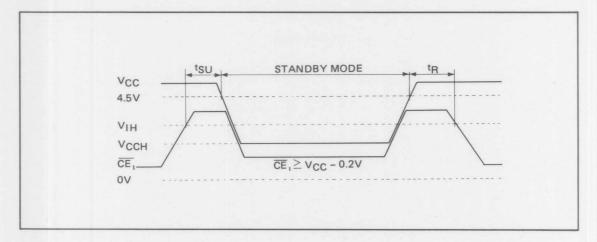


LOW VCC DATA RETENTION CHARACTERISTICS

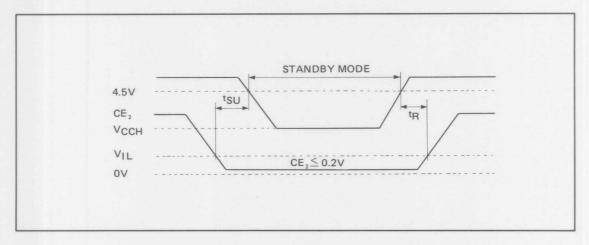
 $(T_a = 0^{\circ}C \text{ to } +70^{\circ}C, \text{ unless otherwise noted})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
V _{CC} for Data Retention	Vccн	2		0	V	$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2\text{V}, \text{CE}_2 \ge \text{V}_{\text{CC}} - 0.2\text{V}$ or $\text{CE}_2 \le 0.2\text{V}$
0 80 0	0011	0	-00	0	WED	$CE_2 \leq 0.2V$
Data Retention Current	ГССН	08		08	mA	$V_{CC} = 3V$, $\overline{CE}_1 \ge V_{CC} - 0.2V$, $CE_2 \ge V_{CC} - 0.2V$ or $CE_2 \le 0.2V$
					A 111	$V_{CC} = 3V, CE_2 \le 0.2V$
CS to Data Retention Time	tsu	0	low CE,	riap of a	ns	Note: 1. A Write Cycle occurs durin 2. OE may be both high and I
Operation Recovery Time	tR	tRC	go rever	VE, which	ns	3. tAS is specified from CE,

CE1 CONTROL



CE, CONTROL



CAPACITANCE

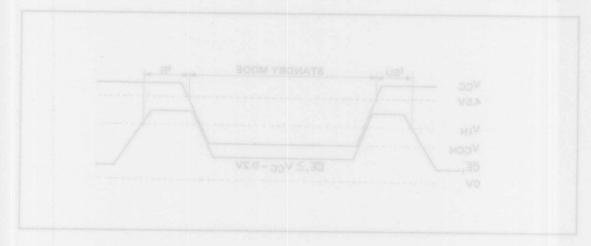
 $(Ta = 25^{\circ}C, f = 1MHz)$

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input/Output Capacitance	C _{I/O}			8	pF
Input Capacitance	CIN			6	pF

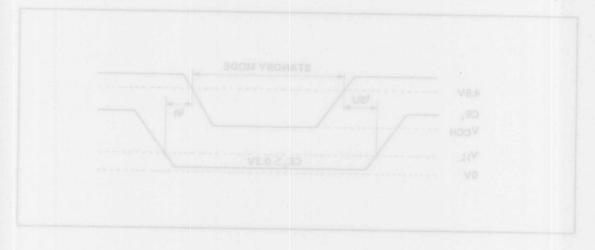
Note: This parameter is periodically sampled and not 100% tested.

9

CE, CONTROL



CE, CONTROL



CAPACITANCE

(E) = 26°C, 1 = 1MH21

Note: This parameter is periodically sampled and not 100% tested.

P

semiconductor

NSM2916RS

1.384-BITS STATIC 16 K MASK ROM (E3-S-023-32)

CENERAL DESCRIPTION

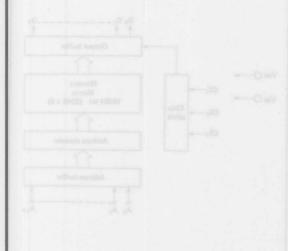
to MSM2916RS is a 16,384-bits static, N channel MOS Read only memory organized as 2,048 words by 8 bits. The three-state outputs and TTL inputs/outputs level allow for direct interface with common system bus structures. The MSM2916RS single 15 V power supply and 250 ns access time are both ideal for usage with high performance.

three chip selects CS1, CS2 and CS2 may be defined by customer and fixed during the madking process.

EATURES

MOS MASK ROMS

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

(Top Vlaw)

A,C 1 2ADVCC

A,C 2 235A,

A,C 3 205A,

A,C 4 2105A,

A,C 5 2005A,

A,C 6 19DA,

A,C 6 19DA,

A,C 7 18DCS,

B,C 7 18

CS₁, CS₂ and CS₃ are programmable CHIP SELECTS

:efol/

MSM2916RS

16,384-BITS STATIC 16 K MASK ROM (E3-S-023-32)

GENERAL DESCRIPTION

The MSM2916RS is a 16,384-bits static, N channel MOS Read only memory organized as 2,048 words by 8 bits. The three-state outputs and TTL inputs/outputs level allow for direct interface with common system bus structures. The MSM2916RS single +5 V power supply and 250 ns access time are both ideal for usage with high performance microcomputers.

The three chip selects CS₁, CS₂ and CS₃ may be defined by customer and fixed during the masking process.

FEATURES

• Organization	2048W x 8 bit
Static Operation	
Supply Voltage	5V ± 10%
• Access Time	250 ns Max.
• Power Dissipation	550 mW Max.

• Input Voltage	VIH = 2.0V Min.,
	VIL = 0.8V Max.
Output Voltage	VOH = 2.4V Min.,
	Vol = 0.4V Max

Package 24 PIN DIP



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

A₀ 2 23 A₈
A₅ 3 22 A₉
A₄ 4 21 C₉
A₅ 5 20 C₅
A₇ 6 19 A₁₀
A₁ 7 18 C₅
A₀ 8 17 D₇
D₀ 9 16 D₆
D₁ 10 15 D₅
D₁ 11 14 D₄

VSSC 12

Note:

 ${\rm CS_1}$, ${\rm CS_2}$ and ${\rm CS_3}$ are programmable CHIP SELECTS

13 D₃

Vcc O

Vss O

CS1

Chip select

CS3

Address decoder

Address buffer

9

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	V
Input Voltage	VI	-0.3 to +7.0	V
Output Voltage	Vo	-0.3 to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
"H" Input Voltage	V _{IH}	2.0		Vcc	V
"L" Input Voltage	VIL	-0.3		0.8	V

DC CHARACTERISTICS

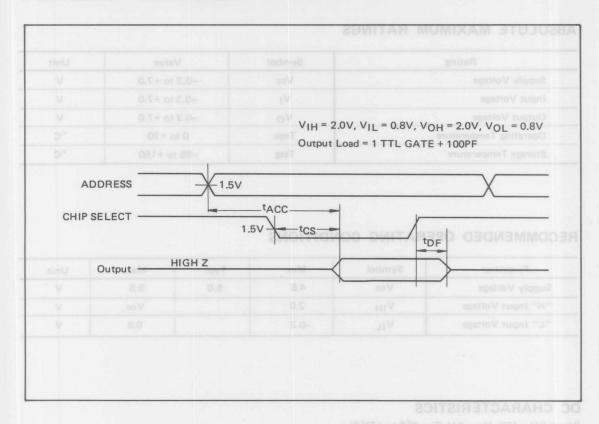
 $(Vcc = 5 V \pm 10\%, Vss = 0 V, Ta = 0^{\circ}C to +70^{\circ}C)$

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
"H" Input Voltage	VIH		2.0		Vcc	V
"L" Input Voltage	VIL		-0.3		0.8	V
"H" Output Voltage	Vон	I _{OH} = -100μA	2.4			V
"L" Output Voltage	VOL	I _{OL} = 1.6 mA			0.4	V
Input Leak Current	ILI	V ₁ = 0 ~ Vcc	-10		10	μΑ
Output Leak Current	ILO	V _O = 0 ~ Vcc	-10		10	μΑ
Power Supply Current	Icc	Vcc = 5.5V			100	mA
Input Capacitance	CI	V _I = 0V, V _O = 0V f = 1 MHz			6	pF
Output Capacitance	CO	Ta = 25°C			12	pF

AC OPERATING CHARACTERISTICS

 $(Vcc = 5 V \pm 10\%, Vss = 0 V, Ta = 0^{\circ}C to +70^{\circ}C)$

Parameter	Symbol	Min.	Max.	Unit
Read Cycle time	tCYC	250		ns
Address Access time	tACC		250	ns
Chip Select Access time	tCS		150	ns
Output Disable Delay time	t _{DF}		150	ns



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MSM2932RS

32,768-BITS STATIC-32K MASK ROM (E3-S-024-32)

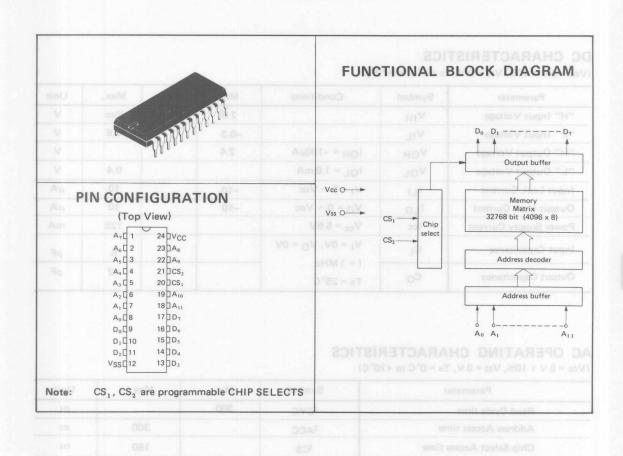
GENERAL DESCRIPTION

The MSM2932RS is a 32,768-bits static, N channel MOS Read only memory organized as 4,096 words by 8 bits. The three-state outputs and TTL inputs/outputs level allow for direct interface with common system bus structures. The MSM2932RS single +5 V power supply and 300 ns access time are both ideal for usage with high performance microcomputers.

The two chip selects CS₁ and CS₂ may be defined by customer and fixed during the masking process.

FEATURES

Organization	4096W x 8 bit	• Input Voltage	V _{IH} = 2.0V Min.,
• Static Operation	No clocks required		VIL = 0.8V Max.
Supply Voltage		Output Voltage	V _{OH} = 2.4V Min.,
• Access Time	300 ns Max.		$V_{OI} = 0.4V \text{ Max.}$
• Power Dissipation	687 mW Max.	Package	24 PIN DIP



q

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	V
Input Voltage	VI	-0.3 to +7.0	V
Output Voltage	Vo	-0.3 to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg annad	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	Sego V
"H" Input Voltage	VIH	2.0	201 1 N	Vcc	V
"L" Input Voltage	V _I L ecos	-0.3		0.8	V

DC CHARACTERISTICS

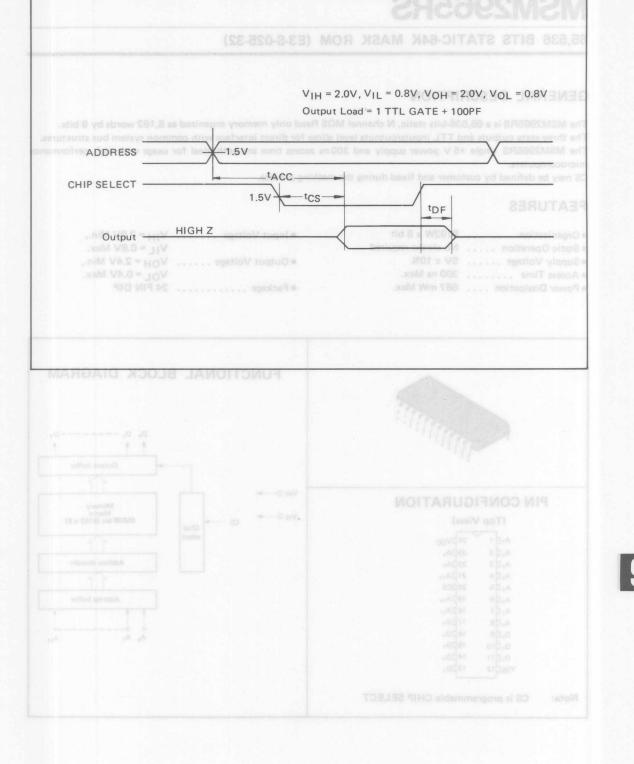
 $(Vcc = 5 V \pm 10\%, Vss = 0 V, Ta = 0^{\circ} C to +70^{\circ} C)$

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
"H" Input Voltage	VIH		2.0		Vcc	V
"L" Input Voltage	VIL		-0.3	Million.	0.8	V
"H" Output Voltage	VOH	I _{OH} = -100μA	2.4	- Alle		V
"L" Output Voltage	VOL	I _{OL} = 1.6 mA			0.4	٧
Input Leak Current	ILI	V ₁ = 0 ~ Vcc	-10	TARILIES A	10	μΑ
Output Leak Current	ILO	V _O = 0 ~ Vcc	-10	1.00	10	μΑ
Power Supply Current	Icc	V _{cc} = 5.5V		(Mark	125	mA
Input Capacitance	CI	V _I = 0V, V _O = 0V f = 1 MHz		ASSES ASSES	6	pF
Output Capacitance	co	$T = TMHZ$ $Ta = 25^{\circ}C$		21 Dass	12	pF

AC OPERATING CHARACTERISTICS

 $(Vcc = 5 V \pm 10\%, Vss = 0 V, Ta = 0^{\circ} C to +70^{\circ} C)$

Parameter	Symbol	Min.	Max.	Unit
Read Cycle time	tCYC	300		ns
Address Access time	tACC		300	ns
Chip Select Access time	^t CS		150	ns
Output Disable Delay time	^t DF		150	ns



MSM2965RS

65,536 BITS STATIC-64K MASK ROM (E3-S-025-32)

GENERAL DESCRIPTION

The MSM2965RS is a 65,536-bits static, N channel MOS Read only memory organized as 8,192 words by 8 bits. The three-state outputs and TTL inputs/outputs level allow for direct interface with common system bus structures. The MSM2965RS single +5 V power supply and 300 ns access time are both ideal for usage with high performance microcomputers.

CS may be defined by customer and fixed during the masking process.

FEATURES

Organization	8192W x 8 bit	● Input Voltage	VIH = 2.0V Min.,
Static Operation	No clocks required		VII = 0.8V Max.
Supply Voltage	5V ± 10%	Output Voltage	VOH = 2.4V Min.,
• Access Time	300 ns Max.		VOL = 0.4V Max.
• Power Dissipation	687 mW Max.	Package	24 PIN DIP



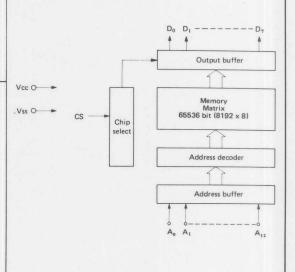
PIN CONFIGURATION

(Top View)

٠.	000		
A ₇ [1	24	Vcc
A ₆	2	23	DA ₈
A ₅	3	22	JA,
A ₄ [4	21	A12
A3 [5	20	cs
A ₂	6	19	A10
AIC	7	18	AII
A ₀	8	17	D 7
DoD	9	16	DD6
DIC	10	15	D ₅
D ₂	11	14	D ₄
VSSI	12	13	Do.

Note: CS is programmable CHIP SELECT

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	V
Input Voltage	VI	-0.3 to +7.0	V
Output Voltage	V _O	-0.3 to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
"H" Input Voltage	VIH	2.0		Vcc	V
"L" Input Voltage	VIL	-0.3		0.8	V

DC CHARACTERISTICS

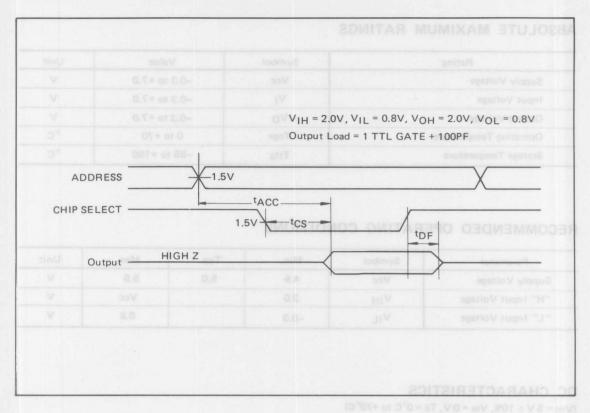
 $(Vcc = 5 V \pm 10\%, Vss = 0 V, Ta = 0^{\circ} C to +70^{\circ} C)$

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
"H" Input Voltage	VIH		2.0		Vcc	V
"L" Input Voltage	VIL		-0.3		0.8	V
"H" Output Voltage	VOH	I _{OH} = -100μA	2.4			V
"L" Output Voltage	VOL	I _{OL} = 1.6 mA			0.4	V
Input Leak Current	ILI	V _I = 0 ~ Vcc	-10		10	μΑ
Output Leak Current	ILO	V _O = 0 ~ Vcc	-10		10	μΑ
Power Supply Current	Icc	V _{cc} = 5.5V			125	mA
Input Capacitance	Cl	V _I = 0V, V _O = 0V f = 1 MHz			6	pF
Output Capacitance	CO	Ta = 25°C			12	pF

AC OPERATING CHARACTERISTICS

 $(Vcc = 5 V \pm 10\%, Vss = 0 V, Ta = 0^{\circ} C to +70^{\circ} C)$

Parameter	Symbol	Min.	Max.	Unit	
Read Cycle time	tCYC	300		ns	
Address Access time	†ACC		300	ns	
Chip Select Access time	tcs		100	ns	
Output Disable Delay time	^t DF		100	ns	



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AC OPERATING CHARACTERISTICS

SM38

OKI semiconductor

MSM3864RS

8,192 WORD x 8 BIT MASK ROM (E3-S-026-32)

GENERAL DESCRIPTION

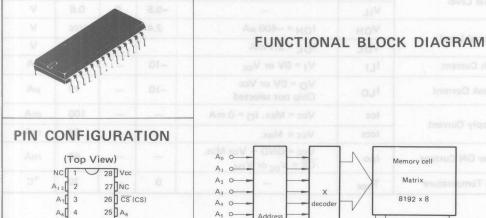
MSM3864RS is an N-channel silicon gate E/D MOS device MASK ROM with a 8,192 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

FEATURES

- 5V single power supply
- 8,192 words x 8 bits
- Access time: 200 ns MAX
- Input/output TTL compatible
- 3-state output

- Power down mode
- 28-pin DIP



A5[

A4[

24 A,

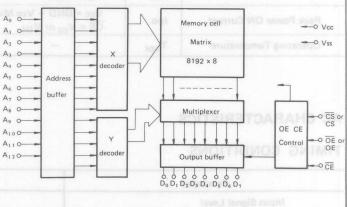
23 A11

21 A10

22 OE (OE)

 $A_0 \sim A_{12}$: Address input $D_0 \sim D_7$: Data output $\overline{\text{CE}}$: Chip enable $\overline{\text{CS}}$: Chip select

Note: Please specify the OE active level and CS active level or open in ordering this IC.



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ABSOLUTE MAXIMUM RATINGS

 $(Ta = 25^{\circ}C)$

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	-0.5 to 7	V	Respect to V _{SS}
Input Voltage	VI	-0.5 to 7	V	Respect to V _{SS}
Output Voltage	Vo	-0.5 to 7	V	Respect to V _{ss}
Power Dissipation	PD	EAM solved design MAS	W	Per package
Operating Temperature	Topr	0 to 70	°C	operates on a 5V single power
Storage Temperature	T _{stg}	-55 to 150	°C	supplied of an asynchronous

OPERATING CONDITION AND DC CHARACTERISTICS

D	Complete	Manusina Candida		Unit			
Parameter	Symbol	Measuring Condition	Min.	Тур.	Max.	Offic	
Room Sanda Walters	V _{cc}	- Tuqtuo state-E	4.5	5	5.5	V	
Power Supply Voltage	V _{SS}		0	0	0	V	
I CiI II	VIH		2	5	6	V	
Input Signal Level	VIL	-	-0.5	0	0.8	V	
Output Signal Lavel	Voн	ΙΟΗ = -400 μΑ	2.4	-	Vcc	V	
Output Signal Level	VOL	I _{OL} = 2.1 mA		1-	0.4	V	
Input Leak Current	ILI	V _I = 0V or V _{CC}		14/	10	μΑ	
Output Leak Current	ILO	V _O = 0V or Vcc Chip not selected		-	10	μΑ	
Davies Supply Courses	Icc	Vcc = Max. I _O = 0 mA	-	-	100	mA	
Power Supply Current	Iccs	Vcc = Max.	WO11	Afilu	30	mA	
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. CE = V _{cc} or V _{IH}	-	-(see	60	mA	
Operating Temperature	Topr	A	0	27 [100	70	°C	

AC CHARACTERISTICS

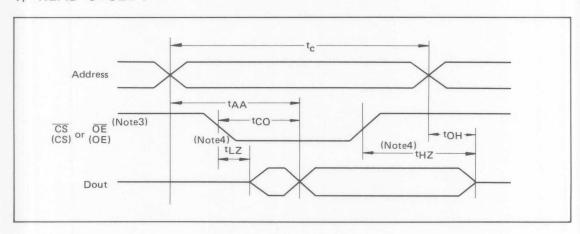
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V _{IH} =2.0V V _{IL} =0.8V
Input Rising, Falling Time	tr=ty=15 ns
Timing Manual District	Input Voltage=1.5V
Timing Measuring Point Voltage	Output Voltage=0.8V & 2.0V
Loading Condition	C _L =100 pF + 1 TTL

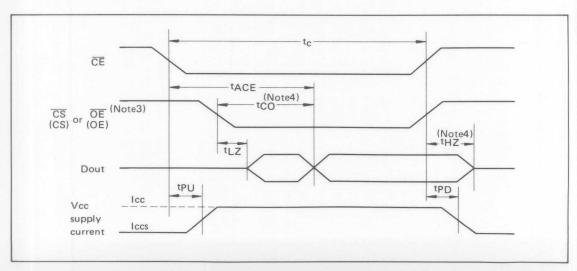
READ CYCLE

Total is tradit salacido.		Spec	cification \	Value	original beautiful	ntimetals and (b)
Parameter	Symbol	Min.	Тур.	Max.	Unit	Remarks
Cycle Time	t _C	200	ting and a	dall lime s	ns	While, the show
Address Access Time	tAA	_	_	200	ns	
Chip Enable Access Time	†ACE	-	-	200	ns	
Output Delay Time	tco	-	-	100	ns	NPUT/OUTPUT CAI
Output Setting Time	tLZ	10		_	ns	14 = 25°C, f = 1 MHz)
Output Disable Time	tHZ	0	-	100	ns	
Output Retaining Time	tOH	10	Specifical series	-	ns	
Power Up Time	tpU	0	7 -	100	ns	Parameter
Power Down Time	tPD	-	-	100	ns	Input Canadiance

1) READ CYCLE-1 (1)



2) READ CYCLE-2(2)



Note: (1) \overline{CE} is "L" level.

(2) The address is decided at the same time as or ahead of CE "L" level.

(3) The OE and CS are shown in the negative logic here, however the active level is freely selected.
(4) t_{Lz} is determined by the later level, CE "L"/CS "L" or OE "L".
t_{Hz} is determined by the earlier CE "H"/CS "H" or OE "H".

While, tHz shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Specification Value		Unit	Remarks	
		Min.	Max.	Fl.dt	smiT qU rawo	
Input Capacitance	CI	D1 -	8	pF	VI=0V	
Output Capacitance	CO		10	pF	V _O =0V	

MSM38128RS

16384 WORD x 8 BIT MASK ROM (E3-S-027-32)

GENERAL DESCRIPTION

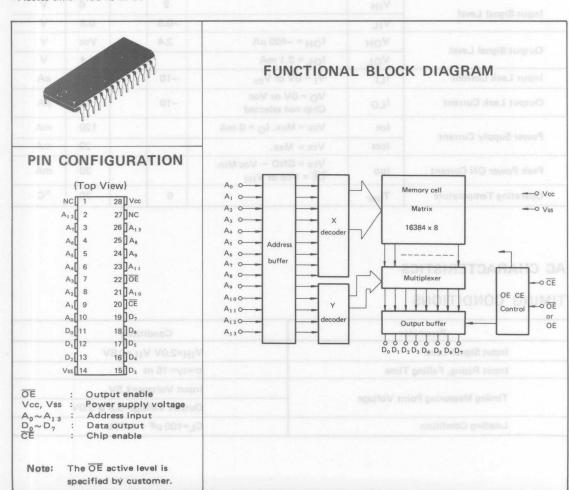
MSM38128RS is an N-channel silicon gate E/D MOS device ROM with a 16,384 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 20 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

Since it provides both CE and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

FEATURES

- 16384 words x 8 bits
- 5V single power supply
- Access time: 450 ns MAX
- Input/output TTL compatible
- 3-state output

- Power down mode
- 28-pin DIP



ABSOLUTE MAXIMUM RATINGS

 $(Ta = 25^{\circ}C)$

Rating	Symbol	Value	Unit	Conditions	
Power Supply Voltage	Vcc	-0.5 to 7	V	Respect to V _{SS}	
Input Voltage	VI	-0.5 to 7	V		
Output Voltage	Vo	-0.5 to 7	V		
Operating Temperature	Topr	0 to 70	°C	28RS is an N-channel	
Storage Temperature	T _{stg}	-55 to 150	°C	gle power supply and	

OPERATING CONDITION AND DC CHARACTERISTICS

					Linia	
Parameter	Symbol	Measuring Condition	Min.	Тур.	Max.	Unit
Davis Const. Walter mos	V _{cc}	Input/output TTL compatible	4.5	5	5.5	V
Power Supply Voltage	V _{SS}	3-state output	0	0	0	V
Input Signal Level	VIH		2	AANA a	6	V
	VIL		-0.5		0.8	V
Output Signal Level	Voн	I _{OH} = -400 μA	2.4	ad Obs	Vcc	V
	VOL	I _{OL} = 2.1 mA			0.4	V
Input Leak Current	1LI	V _I = 0V or V _{CC}	-10		10	μΑ
Output Leak Current	ILO	V _O = 0V or Vcc Chip not selected	-10		10	μΑ
D	Icc	Vcc = Max. I _O = 0 mA			120	mA
Power Supply Current	Iccs	Vcc = Max.			20	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. CE = Vco or VIH	MUII	AHU	20	mA
Operating Temperature	Topr		0	asville	70	°C

AC CHARACTERISTICS

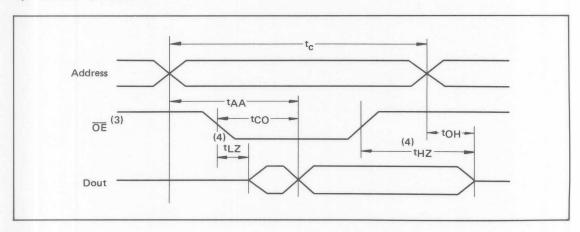
TIMING CONDITIONS

Parameter	Conditions			
Input Signal Level	V _{IH} =2.0V V _{IL} =0.8V			
Input Rising, Falling Time	tr=ty=15 ns			
Timing Manusing Deine Walters	Input Voltage=1,5V			
Timing Measuring Point Voltage	Output Voltage=0.8 & 2.0V			
Loading Condition	C _L =100 pF + 1 TTL			

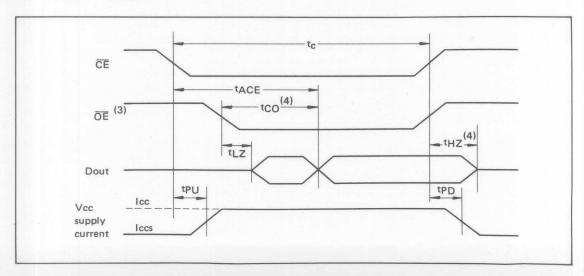
READ CYCLE

ely selected.	at at level out	Spec	cification \	Value	Unit	The second secon
Parameter	Symbol	Min.	Тур.	Max.		Remarks
Cycle Time	t _c	450	al ri arch	arti gnite	ns	this shows time
Address Access Time	tAA			450	ns	
Chip Enable Access Time	†ACE			450	ns	
Output Delay Time	tco			150	ns	NPUT/OUTPUT CAL
Output Setting Time	tLZ	20			ns	To = 25°C, f = 1 MHz)
Output Disable Time	tHZ	0		120	ns	
Output Retaining Time	tOH	20	Specifical		ns	Parameter
Power Up Time	tPU	0		120	ns	1939(1636-1
Power Down Time	tPD			120	ns	Jeout Canadiance

1) READ CYCLE-1(1)



2) READ CYCLE-2⁽²⁾



- Note: (1) CE is "L" level.
 - (2) The address is decided at the same time as or ahead of $\overline{\text{CE}}$ "L" level.
 - (3) OE is shown in the negative logic here, however the active level is freely selected.
 - (4) tco and tLZ are determined by the later CE "L" or OE "L".

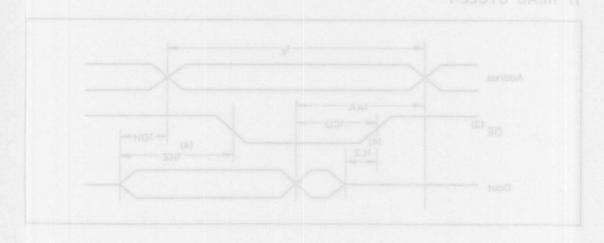
tHz is determined by the earlier $\overline{\text{CE}}$ "H" or $\overline{\text{OE}}$ "H".

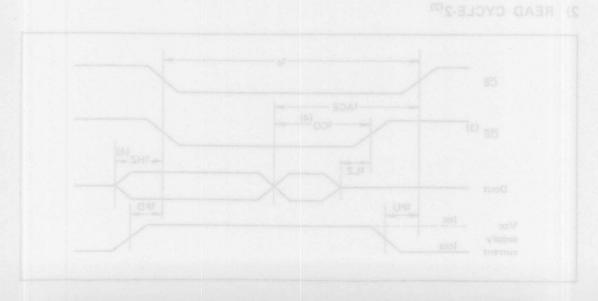
tHz shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter S	Symbol	Specification Value		Unit	Remarks
	en (Min.	Max.	Ugi	ower Up Time
Input Capacitance	CI		8	pF	V _I =0V
Output Capacitance	CO		10	pF	V _O =0V





OKI semiconductor

MSM38128ARS

16,384 WORD x 8 BIT MASK ROM (E3-S-028-32)

GENERAL DESCRIPTION

MSM38128ARS is an N-channel silicon gate E/D MOS device MASK ROM with a 16,384 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

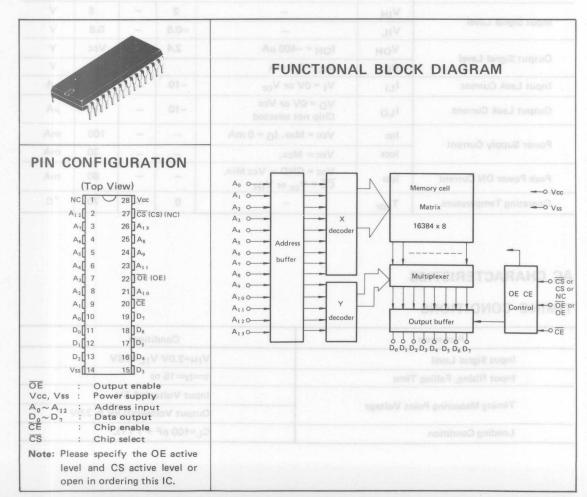
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

FEATURES

- 5V single power supply
- 16384 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- Power down mode

• 3-state output

• 28-pin DIP



ABSOLUTE MAXIMUM RATINGS

 $(Ta = 25^{\circ}C)$

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	-0.5 to 7	V	Respect to V _{SS}
Input Voltage	VI	-0.5 to 7	V	Respect to V _{SS}
Output Voltage	Vo	-0.5 to 7	V	Respect to V _{SS}
Power Dissipation	PD	1	W	Per package
Operating Temperature	Topr	0 to 70	°C	Mobile SA HS is an IN-chant
Storage Temperature	T _{stg}	-55 to 150	°C	ption of an asynchronous

OPERATING CONDITION AND DC CHARACTERISTICS

2	0	Manusian Canditi		Rating		Unit
Parameter	Symbol	Symbol Measuring Condition		Тур.	Max.	Unit
abom myob t	V _{cc}	V _{cc} –		5	5.5	V
Power Supply Voltage	V _{SS}		0	0	0	V
	VIH		2	-	6	V
Input Signal Level	VIL		-0.5	-	0.8	V
0 0	Vон	ΙΟΗ = -400 μΑ	2.4	-	Vcc	V
Output Signal Level	VOL	I _{OL} = 2.1 mA		-	0.4	V
Input Leak Current	ILI	V _I = 0V or V _{CC}	-10	-	10	μΑ
Output Leak Current	ILO	V _O = 0V or Vcc Chip not selected	-10	-	10	μΑ
D	Icc	Vcc = Max. I _O = 0 mA	-	-	100	mA
Power Supply Current	Iccs	Vcc = Max.	1500	TA (1)	30	mA
Peak Power ON Current	Ipo	$\frac{\text{Vcc} = \text{GND} \sim \text{Vcc Min.}}{\text{CE}} = \text{V}_{\text{cc}} \text{ or V}_{\text{IH}}$	-	- Con	60	mA
Operating Temperature	Topr		0	# <u>W</u> [85	70	°C

AC CHARACTERISTICS

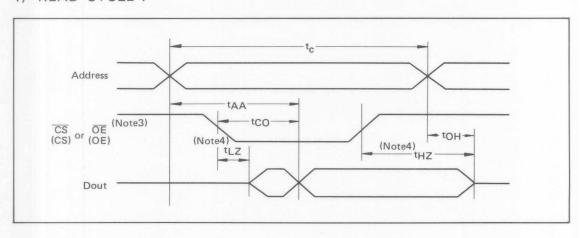
TIMING CONDITIONS

Parameter	Conditions		
Input Signal Level	V _{IH} =2.0V V _{IL} =0.8V		
Input Rising, Falling Time	tr=ty=15 ns		
T:! M	Input Voltage=1.5V		
Timing Measuring Point Voltage	Output Voltage=0.8V & 2.0V		
Loading Condition	C _L =100 pF + 1 TTL		

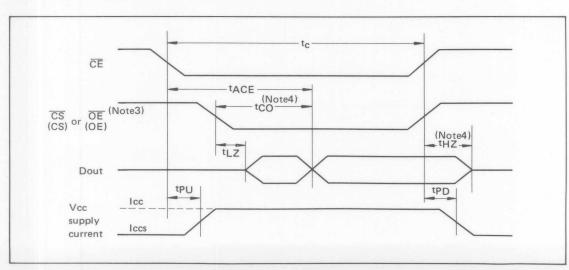
READ CYCLE

Codposite Atlanta in taker a	0 10 70	Spec	ification \	/alue	rit wel ben	mateb short (8)
Parameter	Symbol	Min.	Тур.	Max.	Unit	Remarks
Cycle Time	t _c	250	bns <u>p</u> nita	ont library en	ns	While, the shi
Address Access Time	tAA	-	-	250	ns	
Chip Enable Access Time	†ACE	-	-	250	ns	A C THE THE STREET
Output Delay Time	tco	_	_	100	ns	INPUT/OUTPUT CA
Output Setting Time	tLZ	10	-	-	ns	Tu = 25° C, t = 1 MHz)
Output Disable Time	tHZ	0	_	100	ns	
Output Retaining Time	tOH	10	MINDOGO.	+	ns	Persmeter
Power Up Time	tpU	0	-	100	ns	throught.
Power Down Time	tPD	-	-	100	ns	Input Capacitance

1) READ CYCLE-1 (1)



2) READ CYCLE-2(2)



Note: (1) \overline{CE} is "L" level.

(2) The address is decided at the same time as or ahead of CE "L" level.

(3) The \overline{OE} and \overline{CS} are shown in the negative logic here, however the active level is freely selected.

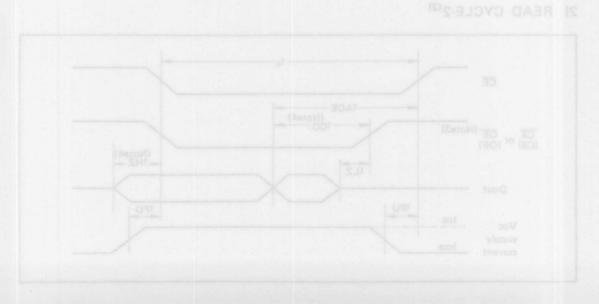
(4) t_{Lz} is determined by the later level, \overline{CE} "L"/ \overline{CS} "L" or \overline{OE} "L". t_{Hz} is determined by the earlier \overline{CE} "H"/ \overline{CS} "H" or \overline{OE} "H".

While, tHz shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Specification Value		Unit	Remarks
	an OI	Min.	Max.	n _{d1}	Power Up Time
nput Capacitance	CI	E	8	pF	V _I =0V
Output Capacitance	CO		10	pF	V _O =0V



OKI semiconductor

MSM38256RS

32768 WORD x 8 BIT MASK ROM (E3-S-029-32)

GENERAL DESCRIPTION

MSM38256RS is an N-channel silicon gate E/D MOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

Since it provides CE, CS and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

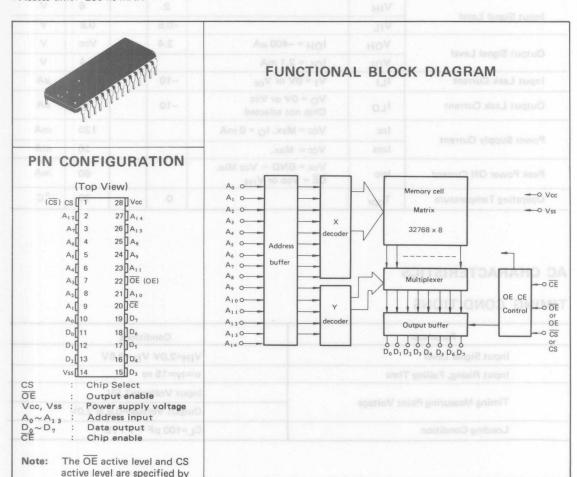
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 250 ns MAX

customer.

- Input/output TTL compatible
- 3-state output

- Power down mode
- 28-pin DIP



ABSOLUTE MAXIMUM RATINGS

 $(Ta = 25^{\circ}C)$

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	-0.5 to 7	V	
Input Voltage	VI	-0.5 to 7	V	Respect to VSS
Output Voltage	Vo	-0.5 to 7	V	
Operating Temperature	Topr	0 to 70	°C	ASM38255RS Is an N-channel
Storage Temperature	T _{stg}	-55 to 150	°C	BV single power supply and

OPERATING CONDITION AND DC CHARACTERISTICS

				11-:4		
Parameter	Symbol	Symbol Measuring Condition		Min. Typ.		Unit
Davies Const. Valtage	V _{cc}	input/output TTL compatible	4.5	5	5.5	V
Power Supply Voltage	V _{SS}	3-stan output	0	0	0	V
Innut Cinnal Laval	VIH		2	2000	6	V
Input Signal Level	VIL		-0.5		0.8	V
Output Signal Laval	Voн	I _{OH} = -400 μA	2.4		Vcc	V
Output Signal Level	VOL	I _{OL} = 2.1 mA			0.4	V
Input Leak Current	ILI	V _I = 0V or V _{CC}	-10	11773	10	μΑ
Output Leak Current	ILO	V _O = 0V or Vcc Chip not selected	-10		10	μΑ
Davies Supply Comment	Icc	Vcc = Max. I _O = 0 mA			120	mA
Power Supply Current	Iccs	Vcc = Max.			30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. CE = Vco or VIH	1015,037	APLUE	60	mA
Operating Temperature	Topr	A	0	mV (6s	70	°C

9

AC CHARACTERISTICS

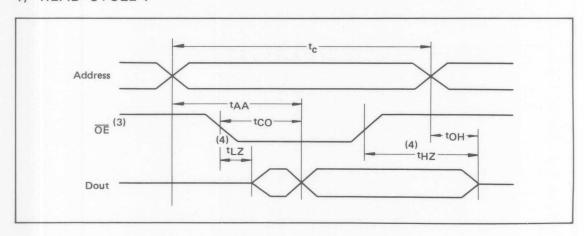
TIMING CONDITIONS

Parameter	Conditions		
Input Signal Level	V _{IH} =2.0V V _{IL} =0.8V		
Input Rising, Falling Time	tr=ty=15 ns		
Timing Magazzing Point Voltage	Input Voltage=1.5V		
Timing Measuring Point Voltage	Output Voltage=0.8 & 2.0V		
Loading Condition	C _L =100 pF + 1 TTL		

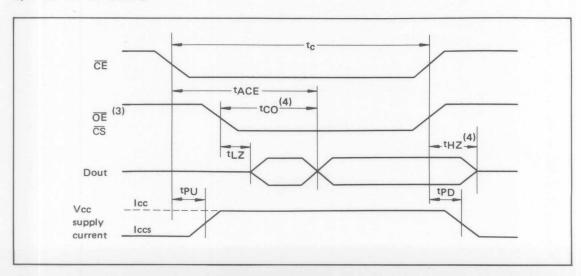
READ CYCLE

ivel is freely selected.	er the active	Spec	ification V	'alue	i nuvorte s	(3) OE and GS and		
Parameter	Symbol	Min.	Тур.	Max.	Unit	Remarks		
Cycle Time	t _c	250	ai si erote		ns	this shows tim		
Address Access Time	tAA			250	ns			
Chip Enable Access Time	tACE			250	ns			
Output Delay Time	tco			100	ns	PUT/OUTPUT CAR		
Output Setting Time	tLZ	10			ns	To = 25°C, 1 = 1 MHz)		
Output Disable Time	tHZ	0		100	ns			
Output Retaining Time	tOH	10	Specifical		ns			
Power Up Time	tpU	0	1		ns	Parametar		
Power Down Time	tPD	0		100	ns	loout Canadiance		

1) READ CYCLE-1 (1)



2) READ CYCLE-2(2)



Note: (1) CE is "L" level.

(2) The address is decided at the same time as or ahead of $\overline{\text{CE}}$ "L" level.

(3) \overline{OE} and \overline{CS} are shown in the negative logic here, however the active level is freely selected.

(4) tco and tLZ are determined by the later CE "L", OE "L" or CS "L".

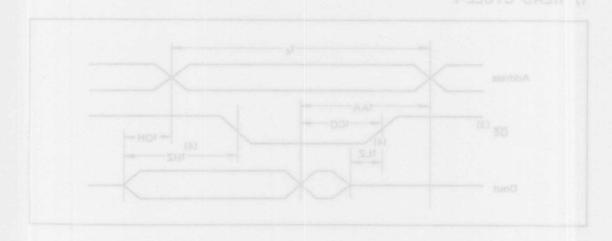
tHz is determined by the earlier $\overline{\text{CE}}$ "H", $\overline{\text{OE}}$ "H" or $\overline{\text{CS}}$ "H".

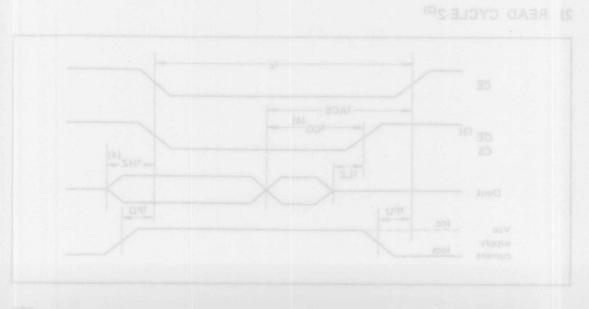
tHz shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	11.		Unit	Remarks
	an an	Min.	Max.	UNI	weer Up Time
Input Capacitance	CI		8	pF	V _I =0V
Output Capacitance	CO		10	pF	V _O =0V





Preliminar

OKI semiconductor

MSM38256ARS

32768 WORD x 8 BIT MASK ROM (E3-S-030-32)

GENERAL DESCRIPTION

MSM38256RS is an N-channel silicon gate E/D MOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

Since it provides both CE and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

FEATURES

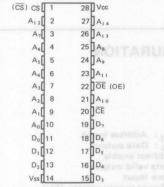
- 32768 words x 8 bits
- 5V single power supply
- Access time: 200 ns MAX
- Input/output TTL compatible
- 3-state output

- Power down mode
- 28-pin DIP



FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION (Top View)



CS : Chip Select

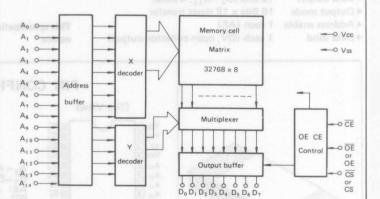
OE : Output enable

Vcc, Vss : Power supply voltage

 $A_0 \sim A_{1 \ 3}$: Address input $D_0 \sim D_7$: Data output CE: Chip enable

Note: The OE active level and CS active level are specified by

customer.



OKI semiconductor

MSM28101AAS

JAPANESE-CHARACTER GENERATING 1M BIT MASK ROM (E3-S-032-32)

GENERAL DESCRIPTION

MSM28101AAS is a 1M Bit Mask ROM using the N channel silicon gate MOS process which stores 3,760 characters of numeric characters, Japanese cursive and square syllabarys, JIS 1st standard Japanese-characters, etc., in one chip.

Since it is of large capacity, Japanese-character pattern of 3,760 characters can be generated with only one chip. Furthermore, since the dot matrix character form of 18 lines x 16 strings is available from the data out pin by only inputting the JIS Japanese-character code into the address pin, it excels in functioning property and proves optimum for constituting the Japanese-character terminal.

The power supply voltage is of 5 V single power supply, the input level is of TTL compatible, the data output is of 3-state output, the data valid is the output of the open collector and is packaged on the 40-pin DIP.

FEATURES

18 x 16 chinese-character font Function

output

Duplex configuration of cell-Configuration

array using the defect permissible

technique

Storage capacity 1082880 Bits

 Number of 3,418 characters

generating characters

Partition 0 ~ 7 and partition Storage

character range 16 ~ 47 of Japanese-character code system for JIS information

processing

Address input

14 Bits $(A_0 \sim A_{13})$ 16 Bits $(\overline{D}_0 \sim \overline{D}_{15}, 3\text{-state})$ Data output Output mode 16 Bits x 18 times transfer

1 each (AE) Address enable

1 each (DV, open collector output) Data valid

1 each $(\phi \tau)$ DC ~ 1.5 MHz · Clock

 Used tempera- $Ta = 0 \sim 70^{\circ}C$

ture

 Access time 10 μs MAX

Data transfer

22 µs/character rate Interface TTL level

Power supply 5V single power supply (±5%)

voltage

· Power con-700 mW TYP

sumption Package

Side-brazed 40-pin DIP

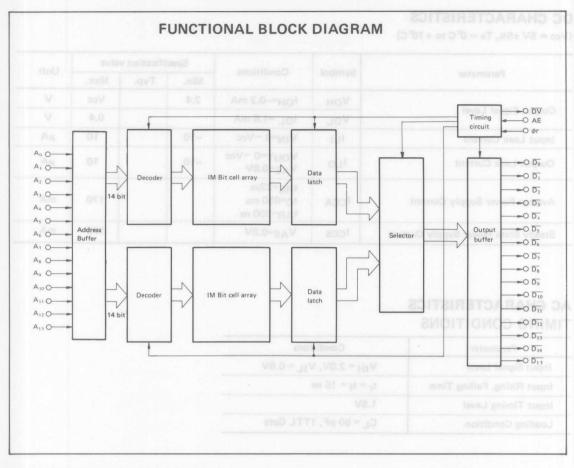
Process E/D MOS process

 Memory cell Multi-gate ROM

This specification is sometimes subject to change without notice



PIN CONFIGURATION (Top View) VSS 1 VSS 2 39 D₁₄ 38 D₁₃ 37 D₁₂ VCC 4 36 D₁₁ $\frac{A_0}{D_0} \sim \frac{A_{13}}{D_{15}}$: Address input Data output A₁₃ PATRITYTYTYTYTY 35 D10 34 Do AE: Address enable A₁₀ A₉ 33 D₈ DV: Data valid output 32 φτ φτ: Clock input A₈ 31 VCC VCC: Power supply voltage (5V) 30 VSS 29 DV 28 D₇ 27 D₆ A₇ VSS: GND (OV) A₆ As A₄ 14 26 D₅ 25 D₄ 24 D₃ A₃ (Note) Connect all VCC and VSS terminals. A₂ 16 A₁ 23 D₂ 22 D₁ A₀ VCC 19 VSS 20 21 Do



ABSOLUTE MAXIMUM RATINGS

 $(Ta = 25^{\circ}C)$

a - 25 C/			100,00	HE THE METER	
Rating	Symbol	Conditions	Value	Unit	
Power Supply Voltage	Vcc	Respect to Vss	-0.5 ~7	V	
Input Terminal Voltage	VIN	Respect to Vss	-0.5 ~7	V	
Output Terminal Voltage	VOUT.	Respect to Vss	-0.5 ~7	V	
Permissible Loss	PD		2 amin 0	W	
Operating Temperature	Topr		0 ~70	°C	
Storage Temperature	T _{stg}		−35 ~ 125		

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Spec	ribity stird To		
			Min.	Тур.	Max.	Unit
Power Supply Voltage	Vcc	5V ± 5%	4.75	5	5.25	Output Vietainin
Power Supply Voltage	Vss		0	0	0	miT p V =2 3/
L C' I I I	VIH	Respect to Vss	2.0	5	6	V
Input Signal Level	VIL	Respect to Vss	-0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

 $(Vcc = 5V \pm 5\%, Ta = 0^{\circ}C to +70^{\circ}C)$

	0	Conditions	Spe	Limit		
Parameter	Symbol	Conditions	Min.	Typ. Max.		Unit
0	Voн	I _{OH} =-0.2 mA	2.4		Vcc	V
Output Signal Level	VOL	I _{OL} =1.6 mA			0.4	V
Input Leak Current	ILI	V _{IN} =0 ~Vcc	-10		10	μΑ
Output Leak Current	ILO	V _{OUT} =0 ~Vcc V _{AE} =0.8V	-10		10	μΑ
Average Power Supply Current	ICCA	t _{RC} =22μs t _C =650 ms t _{AR} =300 ns			170	mA
Steady State Power Supply Current	Iccs	V _{AE} =0.8V			170	mA

AC CHARACTERISTICS

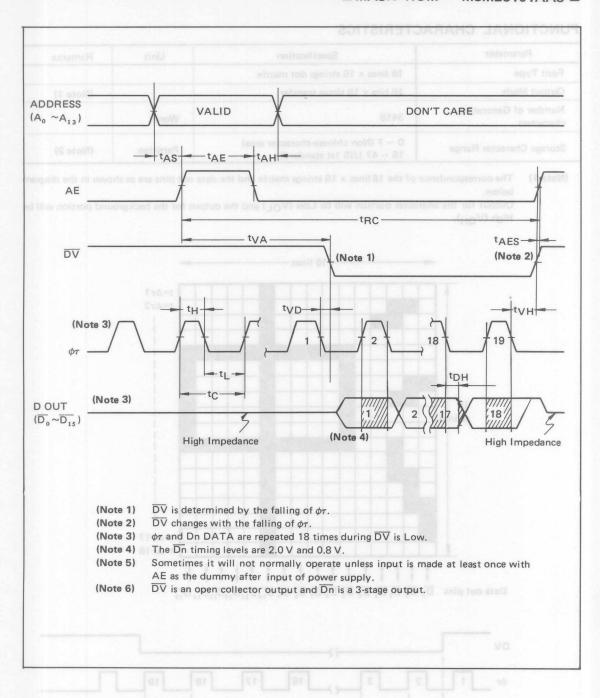
TIMING CONDITIONS

Parameter	Conditions			
Input Signal Level	V _{IH} = 2.0V, V _{IL} = 0.8V			
Input Rising, Falling Time	$t_r = t_f = 15 \text{ ns}$			
Input Timing Level	1.5V			
Loading Condition	C _L = 50 pF, 1TTL Gate			

READ CYCLE

 $(Vcc = 5V \pm 5\%, T_a = 0^{\circ}C \text{ to } +70^{\circ}C)$

Parameter	0-0-1	Conditions	Spe	Llais		
	Symbol		Min.	Тур.	Max.	Unit
Read Cycle Time	tRC	Becomes to Ver	22	v		μS
Address Setting Time	tAS		0		200 A 100 M	ns
AE Pulse Width	tAE		300			ns
Address Retaining Time	^t AH		100		pagalatedian 1	ns
DV Access Time	tVA		- San		10	μS
DV Delay Time	tVD		NAO SI	177 A.O. 190	150	ns
DV Retaining Time	tVH	OFICELL	THOO ON	1 + 2511 21	100	ns
φ _T Pulse Width	SpecH [‡] ation		200			ns
φ _T Delay Time	ay1tL min	- anombnos	450	V8	Parameter	ns
Output Retaining Time	t _{DH}	We LV8	50		agastoV vicini	ns
AE Setting Time	0 tAES 0		0		spatioV vigae	ns



INPUT/OUTPUT CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1 MHz)$

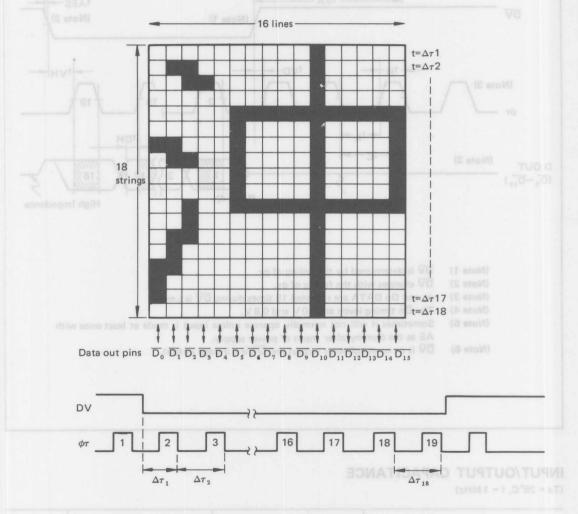
Parameter Parameter	Symbol	Conditions	Specification value			(Note 2)
			Min.	Тур.	Max.	Unit
Input Capacitance (excluding AE)	CIN	V _{IN} = ov	nosež-		8	pF
Input Capacitance (AE terminal)	CIN	V _{IN} = OV	[Nod]	ig fq	15	pF
Output Capacitance	COUT	Vout = 0V	nA.	A RIA	8	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Specification	Unit	Remarks
Font Type	18 lines x 16 strings dot matrix		
Output Mode	16 bits x 18 times transfer		(Note 1)
Number of Generating characters	3418 GLIAV	Word	I _e ,A-,A
Storage Character Range	0 ~ 7 (Non chinese-character area) 16 ~ 47 (JIS 1st standard)	Partition	(Note 2)

(Note 1) The correspondence of the 18 lines x 16 strings matrix and the data out pins are as shown in the diagram below.

Output for the character portion will be Low (V_{OL}) and the output for the background portion will be High (V_{OH}) .



(Note 2) The correspondence of the 1st and 2nd bytes of JIS C 6226 and the address pins are as shown below.

JIS C 6226			Seco	and by	te	iV.	1/5	0	- 6	A Fi	rst byte	itanca (tuan
JIS C 6226	b ₇	b ₆	b _s	b ₄	b ₃	b ₂	b ₁	b ₇	b ₆	b _s	b ₄	b ₃	b ₂	b ₁
Address Pin	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A

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OKI semiconductor MSM28201AAS

1M BIT MASK ROM FOR JAPANESE-CHARACTER PATTERN (E3-S-033-32)

GENERAL DESCRIPTION

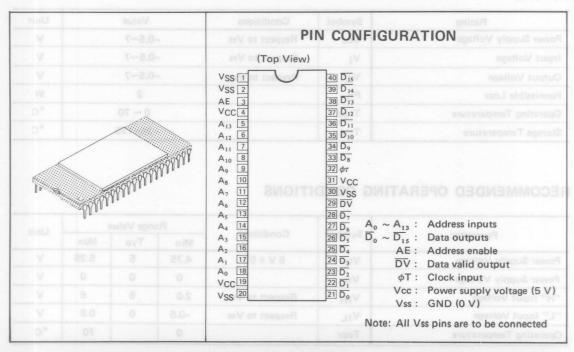
MSM28201AAS is a 1M-bit mask ROM employing an N-channel silicon gate MOS process, and with 3760 Japanese-characters (kanji conforming with JIS no. 2 standards) incorporated in single chip.

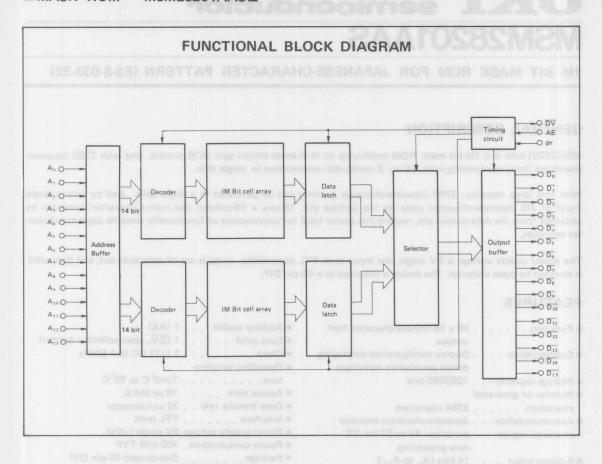
With this large capacity, 3760 Japanese-character patterns can be generated in a single chip. And by only a single input of JIS Japanese-character code via the address pin, 18-row x 16-column dot matrix character forms can be obtained from the data output pin, making this device ideal for construction of functionally versatile Japanese-character terminals.

The power supply voltage is 5V single, the input level TTL compatible, outputs are tri-state data out, and data valid is denoted by open collector. The device is mounted in a 40-pin DIP.

FEATURES

● Function 18 x 16 chinese-character font output	 Address enable 1 (AE) Data valid 1 (DV, open collector output)
Configuration Duplex configuration employing defect permissible technique	 Clock 1 (φT) DC to 1.5MHz Operating tempera-
Storage capacity 1082880 bits Number of generated characters 3384 characters	ture Ta=0°C to 70°C • Access time 10 μs MA X. • Data transfer rate 22 μs/character
Accommodation Japanese-character encoded character region partitions 48 to 87 for JIS data processing.	Interface TTL level Power supply voltage 5V single (±5%) Power consumption . 700 mW TYP
 Address input 14 bits (A₀ to A₁₃) Data output 16 bits (D	Package Side-brazed 40-pin DIP Process E/D MOS process Memory cell





ABSOLUTE MAXIMUM RATINGS

 $(Ta = 25^{\circ}C)$

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	-0.5~7	V
Input Voltage	VI	Respect to Vss	-0.5~7	V
Output Voltage	Vo	Respect to Vss	-0.5~7	V
Permissible Loss	PD	V58 [2]	2	W
Operating Temperature	Topr	Voc[3]	0 ~ 70	°C
Storage Temperature	Tstg	第12	-35~125	°C

RECOMMENDED OPERATING CONDITIONS

Address inputs	Symbol	Conditions	R	ange Valu	е	Unit
Parameter	Symbol	Conditions	Min	Тур	Max	Oili
Power Supply Voltage	Vcc	5 V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss	As West	0	0	0	V
"H" Input Voltage	VIH	Respect to Vss	2.0	5	6	V
"L" Input Voltage	VIL	Respect to Vss	-0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 5\%, Ta = 0^{\circ} C \text{ to } +70^{\circ} C)$

D	Complete	Conditions	F	Range Valu	ie	11-1
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
"H" Output Voltage	Vон	I _{OH} 0.2 mA	2.4		Vcc	V
"L" Output Voltage	VOL	I _{OL} = 1.6 mA	I SAI		0.4	V
Input Leak Current	ILI	V _I = 0 ~ V _{CC}	-10		10	μΑ
Output Leak Current	ILO	V _O = 0 ~ V _{CC} V _{AE} = 0.8V	-10		10	μΑ
Average Power Supply Current	ICCA	$t_{RC} = 22\mu S$, $t_{C} = 650 \text{ ns}$ $t_{AE} = 300 \text{ns}$			170	mA
Rated Power Supply Current	Iccs	V _{AE} = 0.8V			170	mA

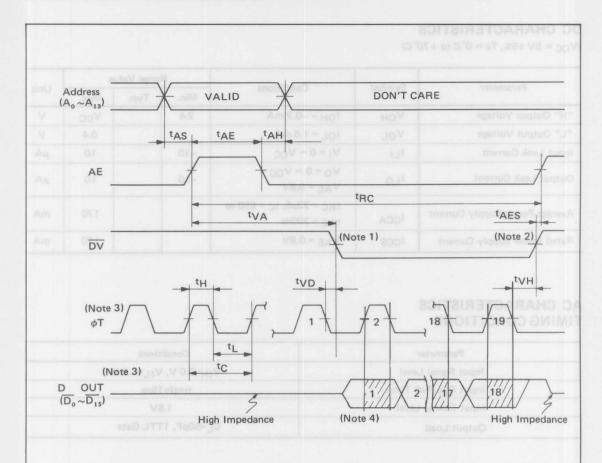
AC CHARACTERISTICS TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V _{IH} =2.0 V, V _{IL} =0.8 V
Input Rise/Fall Time	tr=tf=15ns
Input Timing Level	1.5V
Output Load	C _L =50pF, 1TTL Gate

READ CYCLE

 $(V_{CC} = 5V \pm 5\%, Ta = 0^{\circ} C \text{ to } +70^{\circ} C)$

Parameter	Complete	Canditiana	Spe	cification Va	lue	I I=:
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Uni
Read Cycle Time	tRC	it, and Do the till	22	nego assons	6. VQ8	μS
Address Setting Time	tAS		0			ns
AE Pulse Width	tAE		300			ns
Address Retaining Time	tAH		100			ns
DV Access Time	tvA				10	μS
DV Delay Time	tVD		3000	AHJAYA	150	ns
DV Retaining Time	tvH				100	ns
φ _T Pulse Width	tH		200			ns
φ _T Delay Time	tL	Conditions	450		Paramater	ns
Output Retaining Time	^t DH	V 0=įV	50	(BA gnib	ditance (exclu	ns
AE Setting Time	tAES	V 0=(V	0	(n)	citance (AE p	ns



- **NOTE:** 1. \overline{DV} is determined by the ϕT falling edge.
 - 2. $\overline{\text{DV}}$ is changed by the ϕT falling edge.
 - 3. ϕT and DnDATA are repeated 18 times when \overline{DV} is low.
 - 4. Dn timing levels of 2.0V and 0.8V.
 - 5. Normal operation may not be possible unless there is at least one AE dummy input after the power is switched on.
 - 6. $\overline{\text{DV}}$ denotes open collector output, and $\overline{\text{Dn}}$ the tristate output.

INPUT/OUTPUT CAPACITANCE

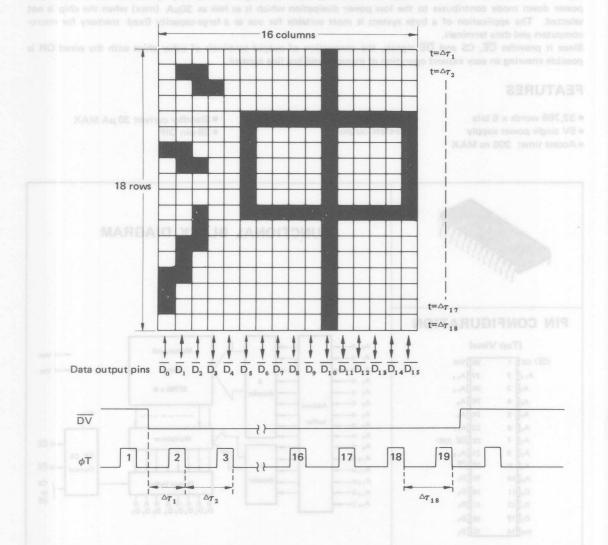
(Ta=25°C, f=1 MHz)

	Parameter	Cumbal	Candiaiaaa	F	Range Valu	ie e	
sn	rarameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Input Ca	pacitance (excluding AE)	CI	V _I =0 V	107		15	pF
Input Ca	pacitance (AE pin)	CI	V ₁ =0 V	SBAT		35	pF
Output (Capacitance	co	V _O =0 V			10	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Range	Unit	Remarks
Font Format	18-row x 16-column dot matrix	0 110 0 X	Unun o
Output Mode	16 bit x 18 transfers		(Note 1)
Number of Characters Generated	3384	Word	30 1000
Character Accommodation Region	48~87 (JIS No.2 standard)	Partition	(Note 2)

Note 1. The relation between the 18-row x 16-column matrix and the data output pins is outlined below. The output is low (VOL) for the character portion, and high (VOH) for the background area.



Note 2. The address pins are related to the JIS C6226 no.1 and no.2 bytes in the following way.

			N	o.2 by	te					N	o.1 by	tes		
JIS C 6226	b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b
Address Pin	A ₁₃	A ₁₂	A ₁₁	A 10	A,	A ₈	A,	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A

OKI semiconductor

MSM53256RS

32,768 WORD x 8 BIT MASK ROM (E3-S-031-32)

GENERAL DESCRIPTION

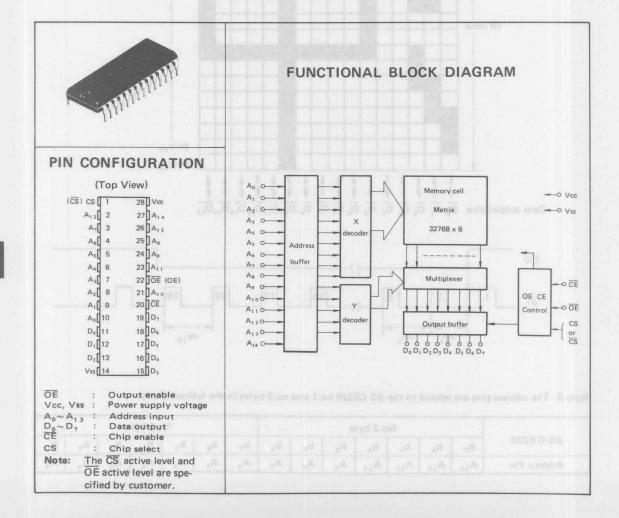
MSM53256AS/RS is a silicon gate C-MOS device ROM with a 32,768 words x 8 bit capacity. It operates on a 5 V single power supply and all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30μ A (max) when the chip is not selected. The application of a byte system is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

Since it provides \overline{CE} , CS and \overline{OE} signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

FEATURES

- 32,768 words x 8 bits
- 5V single power supply
- Access time: 200 ns MAX
- Input/output TTL compatible
- 3-state output

- Standby current 30 µA MAX
- 28-pin DIP



M.L. semiconductor

INSM2708AS

192-BIT UV ERASABLE ELECTRICALLY-PROGRAMMABLE

(E3-S-019-32)

ENERAL DESCRIPTION

to Oki MSM2708 AS (Compatible to the Intal 2708) is a 8192-bit ultraviolet light eraseble and electrically reprosommable EPROM, ideally suited where fast turnstround and gattern experimentation are important requirements, I data inputs and outputs are TTL compatible during both the read and program modes. The outputs are thirdthe, allowing direct interface will common system but structures.

se MSM2708 AS is febricated with the N-channel silicon gate FAMOS technology and is available in a 24-pln dual Hine package.

EATURES

Data Inputs and Outputs TTL Compatible during both Read an

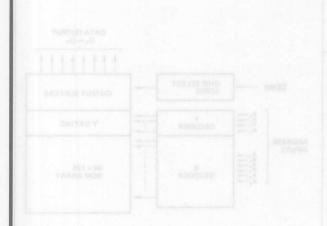
Three-State Outputs — OR-Tie

Static - No Cleate Required

Power Max. Aciess Organization
mW 480 ns 1K x 8

MOS

FUNCTIONAL BLOCK DIAGRAM





MSM2708AS

8192-BIT UV ERASABLE ELECTRICALLY-PROGRAMMABLE READ-ONLY MEMORY

(E3-S-019-32)

GENERAL DESCRIPTION

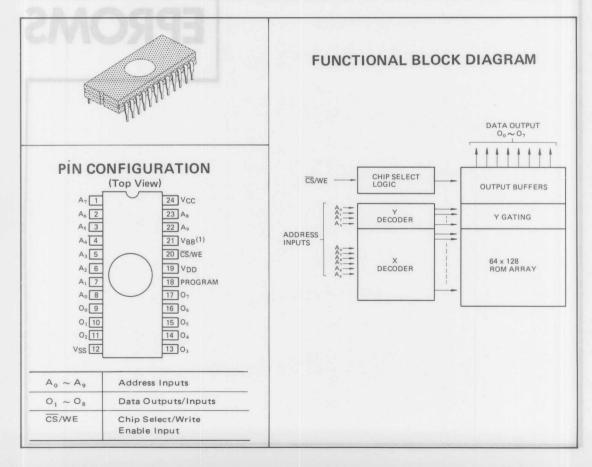
The Oki MSM2708 AS (Compatible to the Intel 2708) is a 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM, ideally suited where fast turnaround and pattern experimentation are important requirements. All data inputs and outputs are TTL compatible during both the read and program modes. The outputs are three-state, allowing direct interface with common system bus structures.

The MSM2708 AS is fabricated with the N-channel silicon gate FAMOS technology and is available in a 24-pin dual in-line package.

FEATURES

- Data Inputs and Outputs TTL Compatible during both Read and Program Modes
- Three-State Outputs OR-Tie Capability
- Static No Clocks Required

TAAA	Max. Power	Max. Access	Organization	
/ISM 2708 AS	800 mW	450 ns	1K x 8	



PIN CONNECTION DURING READ OR PROGRAM

		PIN Number										
Mode	Data I/O 9 ~ 11, 13 ~ 17	Address Inputs 1 ~ 8, 22, 23	V _{SS}	Program 18	V _{DD}	CS/WE	V _{BB}	V _{CC}				
Read	POUT	AIN	GND	GND	+12	VIL	-5	+5				
Deselect	High Impedance	Don't Care	GND	GND	+12	VIH	-5	+5				
Program	DIN	AIN	GND	Pulsed 26V	+12	VIHW	-5	+5				

ABSOLUTE MAXIMUM RATINGS*

• Temperature Under Bias					25°C to +85°C
Storage Temperature					
V _{DD} with Respect to V _{BB} .			AS.	VOH2	+20V to -0.3V
 VCC and VSS with Respect to 	VBB				+15V to -0.3V
• All Input or Output Voltages	with Respect	to VBB during	Read		+15V to -0.3V
 CS/WE Input with Respect to 	VBB during F	Programming	VigaV limi	Not rein being	+20V to -0.3V
 Program Input with Respect to 	V _{BB}	apatlav, ylaqır	. Isalawa ba	un loc T _a e 25 E.a	+35V to -0.3V
Power Dissipation		profession vo.		a di consegnit a	1.5W
THE RESERVE TO SERVE THE PARTY OF THE PARTY					

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC AND AC OPERATING CONDITIONS DURING READ

Temperature Range	0°C to 70°C
V _{CC} Power Supply	5V ± 5%
V _{DD} Power Supply	12V ± 5%
V _{BB} Power Supply	-5V ± 5%

READ OPERATION DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Min.	Typ.(2)	Max.	Units	Test Conditions
Address and Chip Select Input Leakage Current	JLI ggv	margot	1 ₈₈ V	10	μΑ	V _{IN} =5.25V or V _{IN} =V _{IL}
Output Leakage Current	ILO	GND	1,000	10	μΑ	V _{OUT} =5.5V, CS /WE=5V
V _{DD} Supply Current	IDD(3)	GND	50	65	mA	Worst Case Supply
V _{CC} Supply Current	1CC(3)	Pulsed	6	10	mA	Currents - All Inputs High:
V _{BB} Supply Current	1BB(3)	26V	30	45	mA	CS/WE=5V; T _a =0°C
Input Low Voltage	VIL	VSS		0.65	V	
Input High Voltage	VIH	3.0		Vcc ⁺¹	V	SOLUTE MAXIMUM
Output Low Voltage	VOL			0.45	V	I _{OL} =1.6mA
Output High Voltage	VOH1	3.7			V	I _{OH} =-100 A
Output High Voltage	VOH2	2.4			V	IOH=-1mA
Power Dissipation	PD			800	mW	Ta=70°C

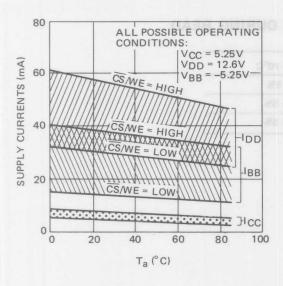
Note: 1. VBB must be applied prior to VCC and VDD. VBB must also be the last power supply switched off.

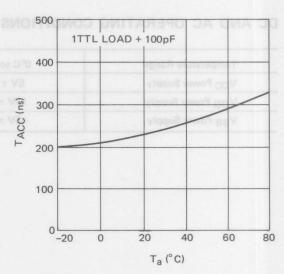
2. Typical values are for $T_a = 25^{\circ}$ C and nominal supply voltages.

3. The total power dissipation is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC} and I_{BB} currents should be used to determine power supply capacity only.

RANGE OF SUPPLY CURRENTS VS. TEMPERATURE

ACCESS TIME VS. TEMPERATURE





A.C. CHARACTERISTICS

Parameter	Symbol	Min.	Тур.	Max.	Units
Address to Output Delay	tACC	400(E ans	350	450	ns manual
Chip Select to Output Delay	tCO	reference to	60	120	ns
Chip Deselect to Output Float	ort effective top	0	hit to abo	120	sixe ns l'angialbas
Address to Output Hold	tон	0	nonnalini	I prevent	O/B A5 window to

CAPACITANCE(1)

 $(Ta = 25^{\circ}C, f = 1 MHz)$

Parameter	Symbol	Тур.	Max.	Unit.	Conditions
Input Capacitance	CIN	4	6	pF	V _{IN} = 0V
Output Capacitance	COUT	8	12	pF	V _{OUT} = 0V

Note: 1. This parameter is periodically sampled and is not 100% tested.

AC TEST CONDITIONS:

Output Load:

1 TTL gate and C_L = 100 pF

Input Rise and

Fall Times: <20 ns

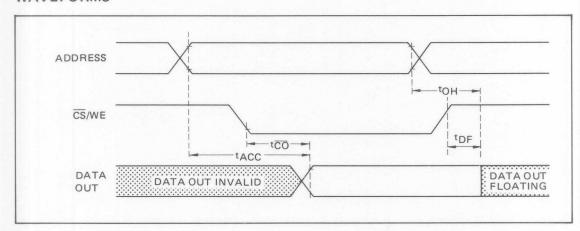
Timing Measurement

Reference Levels: 0.8V and 2.8V for inputs;

0.8V and 2.4V for outputs.

Input Pulse Levels: 0.65V to 2.0V

WAVEFORMS



ERASURE CHARACTERISTICS

The erasure characteristics of the MSM 2708 AS are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4,000 Angstrom (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3,000–4,000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical device in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the MSM 2708 AS is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Oki which should be placed over the MS 3578 AS window to prevent unitentional erasure.

The recommended erasure procedure for the MSM 2708 AS is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x Exposure time) for erasure should be a minimum of 15 W-sec/cm 2 . The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μ W/cm 2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

OKI semiconductor

MSM2716AS

16384-BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE **READ-ONLY MEMORY**

(E3-S-020-32)

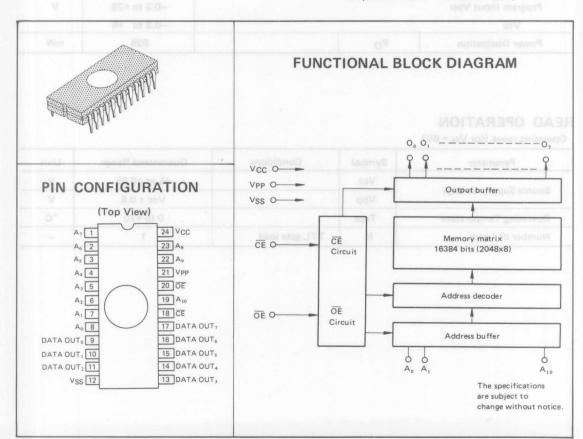
GENERAL DESCRIPTION

The MSM2716AS is a read only memory with the capacity of 2048 words x 8 bits whose contents can be erased by ultraviolet ray irradiation. Since the memory contents can be programmed as desired by the user and the alteration is easy, it is ideal for a processor program.

The MSM2716AS is processed as the N-channel silicon gate MOS with floating gates, and is encased in a standard 24-pin ceramic package.

FEATURES

- Single power supply +5V
- Low power Dissipation 525 mW in operation and 132 mW in standby state
- UV erasable and electrically programmable.
- Minimum programming time 100 seconds for all 16,384 bits.
- Full decoding 2048 words x 8 bits
- Static operation No clock requirement
- TTL connection for inputs/outputs (tristate output)
- Easy expansion of memory capacity (wired-OR connection)



FUNCTION TABLE

Pins	(18)	OE (20)	Vpp (21)	Vcc (24)	OUTPUTS (9~11, 13~17)
Read	VIL	VIL	+5V	+5V	D out
Stand by	VIH	Don't care	+5V	+5V	High Z
Program	Pulsed V _{IL} to V _{IH}	VIH	+25V	+5V	D in
Program Verify	VIL	VIL	+25V	+5V	D out
Program Inhibit	VIL	VIH	+25V	+5V	High Z

High Z = High Impedance

ABSOLUTE MAXIMUM RATING

Rating	Symbol	Conditions	Value	Uni
Storage Temperature	T _{stg}	-	-55 to +125	°C
Terminal Voltage	(netroennos RO-beniw))	(to Vss)	or
Address Input and Data I			-0.3 to +6	
Program Input Vpp			-0.3 to +28	V
Vcc			-0.3 to +6	
Power Dissipation	PD		525	mW

READ OPERATION

Operating range (for Vss = 0V)

Parameter	Symbol	Conditions	Guaranteed Range	Unit
Source Supply Voltage	Vcc		+5 to ±0.25	V
	Vpp	Vas O	Vcc ± 0.6	V
Operating Temperature	Topr		0 to +70	°c
Number of Leads	N	TTL gate load	30 K 1	-

DC OPERATING CHARACTERISTICS

 $(Vcc = 5V \pm 5\%, Vpp = Vcc \pm 0.6V, Ta = 0^{\circ}C \text{ to } +70^{\circ}C \text{ unless specified otherwise})$

Unit Tue et Man District	Complete	Imbot Conditions	Gua	ranteed F	Range	Limite
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Input Leak Current	ILI	V _{IN} = 5.25V		210	10	μΑ
Output Leak Current	ILO	V _{OUT} = 5.25V		1000	10	μΑ
Program Pin Current	Ірр	Vpp = 5.85V		toesse.	5	mA
Collector Supply Current (Standby)	I _{CC1}	CE = V _{IH} , OE = V _{IL}		10	25	mA
Collector Supply Current (Active)	I _{CC2}	OE = CE = VIL		60	100	mA
"H" Input Voltage	VIH	half-num section 2.72 a 2.78	2.2	HISIN:	V _{CC+1}	V
"L" Input Voltage	VIL		-0.1		0.8	V
"H" Output Voltage	Vон	ΙΟΗ = -400 μΑ	2.4	Pareme		V
"L" Output Voltage	VOL	I _{OL} = 2.1 mA			0.45	V

Note: VCC must be supplied before or when Vpp is supplied, and must be cut off when or after Vpp is cut off.

AC OPERATING CHARACTERISTICS

 $(Vcc = 5V \pm 5\%, Vpp = Vcc \pm 0.6V, Ta = 0^{\circ} C to +70^{\circ} C unless specified otherwise)$

2 μ8	Sumah al	Conditions	Gua	araO		
Parameter	Symbol	Conditions	Min.	Тур.	Max. 450 450 120	Unit
Address Output Delay Time	tACC	OE = CE = VIL	81	250	450	ns
CE Output Delay Time	tCE	OE = VIL		280	450	ns
OE Output Delay Time	tOE	CE = VIL		emiT lis	120	ns
Output Disable Delay Time	tDF	CE = VIL	0	amiT saif	100	ns

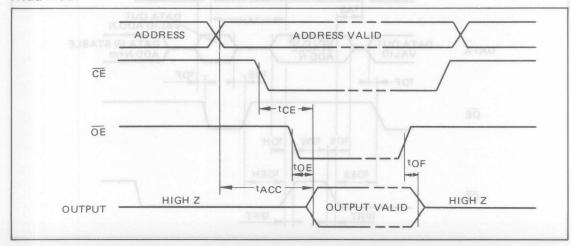
*AC characteristics measuring conditions

Input pulse level 0.8 \sim 2.2V Input rise/fall time Within 20 ns

Output load 1TTL Gate + 100 pF
Timing measurement reference levels Input 1V and 2V, Output 0.8V and 2.4V

TIME CHART

Read Mode



PROGRAMMING OPERATION

(Vcc = 5V \pm 5%, Vpp = 25V \pm 1V, Ta = 25°C \pm 5°C unless specified otherwise)

	0 11	Conditions	Gua	11-1-		
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Input Leak Current	ILI	V _{IN} = 5.25V/0.45V			10	μΑ
Program Pin Current	IPP1	CE = VIL		. 75	6	mA
Programming Current	I _{PP2}	CE = VIH		1131	30	mA
Collector Supply Current	Icc	V00.0 - 99V - 99		3.00	100	mA
"H" Input Voltage	VIH	CCI CE = AIRI OF	2.2	SHOTTUR.	V _{CC+1}	V
"L" Input Voltage	VIL		-0.1		0.8	V

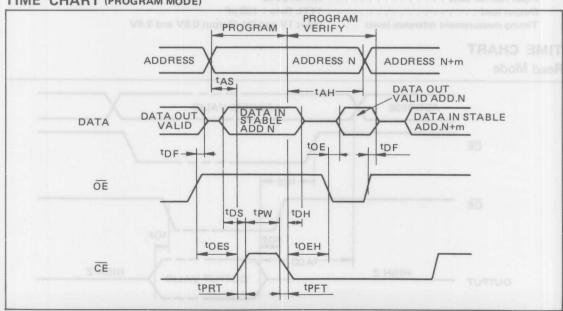
AC CHARACTERISTICS

(Vcc = 5V ± 5%, Vpp = 25V ± 1V, Ta = 25°C ± 5°C unless specified otherwise)

P	Cumphal	Gua	ranteed R	ange	1.1
Parameter	Symbol	Min.	Тур.	Max.	Unit
Address Setup Time	tAS	2	891	Floy Fugi	μS
OE Setup Time	tOES	2	nd bellga	nuar be ta	μS
Data Setup Time	tDS	2			μS
Address Hold Time	^t AH	2	aun n	MITAG	μS
OE Hold Time	tOEH	2	OrmoV =	5%, Vpp	μS
Data Hold Time	tDH	2			μS
Output Disable Delay Time	tDF	0		120	ns
Output Enable Delay Time	tOE	1 n	niT yelet	120	ns
Program Pulse Width	tpW	45	50	55	ms
Program Pulse Fall Time	tPRT 30	5	emiT	pur Deley	ns
Program Pulse Rise Time	tPFT	5	miT yala	I eldssi C	ns

^{*} AC characteristics measurement conditions are the same as those for read operation.

TIME CHART (PROGRAM MODE)



9

OPERATION

Read mode

When \overline{OE} is set to "L" level, reading of the memory contents starts 450 ns (TACC) after the address or 120 ns (tOE) after \overline{OE} if the address is already fixed.

Output deselection

Multiple MSM2716AS chips may be combined by wired-OR connection. The data in one MSM2716AS is read when \overline{OE} is at "L" level. Other MSM2716AS chips are set to the output deselection state by setting the \overline{OE} to the "H" level.

Standby mode

Setting \overline{CE} to "H" level causes the power to be decreased to 1/4 of that in the read mode (525 mW \rightarrow 132 mW).

Programming

All bits of the MSM2716AS are set to "H" level at the time of delivery or after erasure. When 0 is written, the corresponding bit goes to "L" level. In the programming mode, $\overline{\text{OE}}$ input at Vpp=25V is used as "H" level.

The programming data must be supplied in parallel to output pins ($0_{\rm o} \sim 0_{\rm 7}$). The address and input are both TTL level. Supplying $\overline{\rm CE}$ input (TTL "H" level) at 50 ms intervals after setting up the address and data enables programming. Avoid programming by supplying a DC signal to $\overline{\rm CE}$ pin.

Program verify

The MSM2716AS can be verified in the programming mode. Vpp for this operation is 25V.

• Program inhibit

Multiple MSM2716AS chips can be programmed in parallel and with different data in this mode. All pins other than $\overline{\text{CE}}$ can be used in common for all chips.

Supply TTL "H" level to \overline{CE} pins of the chips to be programmed and TTL "L", level to \overline{CE} pins of the chips not to be programmed.

HANDLING OF MSM2716AS

Since the MSM2716AS is an ERROM of N-channel silicon gate FAMOS type, pay special attention as follows in addition to general handling caution of MOS ICs so as to maintain high reliability.

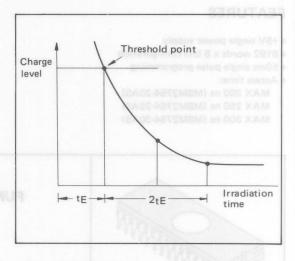
Attention during writing

Since all bits of the MSM2716AS are erased before delivery, writing can be started as it is. Sufficient erasure is necessary before reprogramming.

For writing operation, avoid a location with strong light intensity. 100-200 lux is allowable.

Attention during erasure

The contents of the MSM2716AS can be erased by irradiation of ultraviolet rays. The charge (electrons) in the floating gates decreases with the time lapse, but erasing time te till the threshold point (where all bits are judged as 1 by a writer) is insufficient. Irradiate for another 2 te for sufficient discharge of electrons.



The irradiation energy for erasure of the MSM2716AS contents is 15W-sec/cm².

Caution for handling

- (1) Keep away from carpet or cloth that generates static electricity.
- (2) Perfectly ground the using writer and the system in which the MSM2716AS is used.
- (3) If a soldering iron is used, be sure to ground it.
- (4) Always carry in electrically conductive plastic mat.
- (5) The programmed ROM must be encased in electrically conductive plastic mat.
- (6) Do not touch the glass seal portion with a hand to prevent insufficient erasure caused by decreased UV ray transmission.

Caution for system debugging

Check the functioning status by fluctuating the voltage by $\pm 5\%$.

MSM2764AS

8192 x 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE (E3-S-021-32)

GENERAL DESCRIPTION

The MSM2764AS is a 8192W x 8 bit ultraviolet erassable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM2764AS is ideal for microprocessor programs, etc.

The MSM2764AS is manufactured by the N channel double silicon gate MOS technology and is contained in the 28-pin CERDIP package.

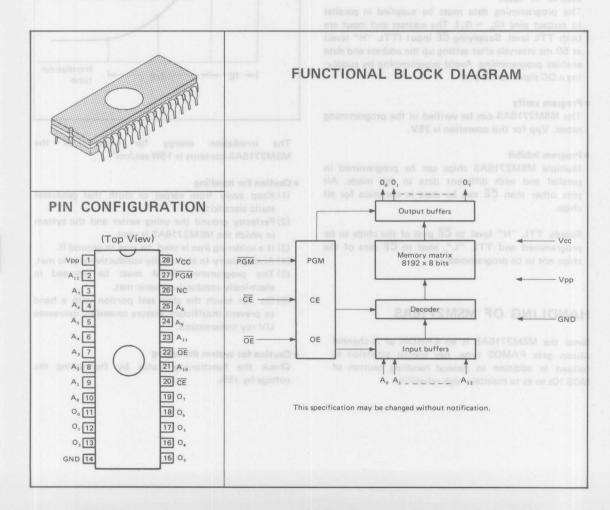
FEATURES

- +5V single power supply
- 8192 words x 8 bits configuration
- 50ms single pulse programming
- Access time:

MAX 200 ns (MSM2764-20AS) MAX 250 ns (MSM2764-25AS) MAX 300 ns (MSM2764-30AS) • Power consumption:

MAX 788 mw (during operation)
MAX 184 mw (during stand-by)

- Perfect static operation
- INPUT/OUTPUT TTL level (tristate output)
- Pin compatible to the INTEL 2764.



FUNCTION TABLE

Pins	(20)	OE (22)	PGM (27)	Vpp (1)	Vcc (28)	Outputs
Read	VIL	VIL	VIH	+ 5V	+5V	Dout
Stand-by	VIH	-	Azere Mil.	+ 5V	+5V	High impedance
Program	VIL	-	VIL	+21V	+5V	DIN
Program Verify	VIL	VIL	VIH	+21V	+5V	Dout
Program Inhibit	VIH	-	J-17 = 30	+21V	+5V	High impedance

^{-;} Can be either VIL or VIH

ABSOLUTE MAXIMUM RATING

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

• Recommended operation condition

Daman at an	Compleal		Limit		Operating	Demonstra	C
Parameter	Symbol	Min	Тур	Max	Temperature	Remarks	Symbo
Vcc Power Supply Voltage	Vcc	4.75	5.0	5.25		emir Helly	V
Vpp Voltage	Vpp	4.15	5.0	5.85	0° C~70° C	Vcc=5V±5%	V pue
"H" Level Input Voltage	VIH	2.00	V, 2V/0	6.25	0 0.370 0	Vpp=Vcc±0.6V	V
"L" Level Input Voltage	VIL	-0.1	-	0.8		TOA	V

The voltage with respect to GND

DC CHARACTERISTICS

 $(Vcc = 5V\pm5\%, Vpp = Vcc\pm0.6V, Ta = 0^{\circ}C\sim70^{\circ}C)$

Boromotor (95)	Symbol	Conditions		Limits		1.1-24
Parameter	Symbol	Conditions	Min.	Stp.	Max.	Unit
Input Leak Current	ILI	V _{IN} = 5.25V		_	10	μΑ
Output Leak Current	ILO	V _{OUT} = 5.25V	11	_	10	μΑ
Vcc Power Current (Stand-by)	Icc ₁	CE = V _{IH}		_	35	mA
Vcc Power Current (Operation)	Icc ₂	CE = VIL	- 10	v -	150	mA
Program Power Current	lpp ₁	Vpp = Vcc±0.6V	_	E/V1	15	mA
Input Voltage "H" Level	VIH		2.0	_	Vcc+1	V
Input Voltage "L" Level	VIL		-0.1	-	0.8	V
Output Voltage "H" Level	Vон	I _{OH} = 400μA	2.4	_	_	V
Output Voltage	VOL	I _{OL} = 2.1mA	TAA N	NIMIX	0.45	٧

AC CHARACTERISTICS

 $(Vcc = 5V\pm5\%, Vpp = Vcc\pm0.6V, Ta = 0^{\circ}C\sim70^{\circ}C)$

	0 1 1	0 111	276	4-20	276	4-25	276	4-30	
Parameter	Symbol	Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Address Access Time	tACC	CE = CE = V _{IL} , PGM = V _{IH}	-	200	-	250	_	300	ns
CE Access Time	^t CE	OE = V _{IL} , PGM = V _{IH}	-	200	ELERIS	250	HO J	300	ns
OE Access Time	CE = V _{IL} , PGM = V _{IH}	10	70	10	100	10	150	ns	
Output Disable Time	tDF	CE = V _{IL} , PGM = V _{IH}	0	60	0	90	0	130	ns

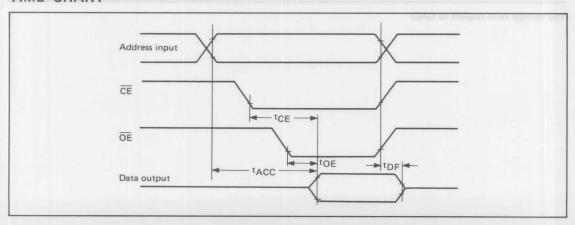
Measurement condition

Input pulse level 0.8V~2.2V Input rise/fall time under 20 ns

Output load 1TTL GATE + 100pF

Output timing reference level Input 1V, 2V/Output 0.8V, 2V

TIME CHART



<PROGRAMMING OPERATION>

DC CHARACTERISTICS

 $(Vcc = 5V\pm5\%, Vpp = 21V\pm0.5V, Ta = 25^{\circ}C\pm5^{\circ}C)$

HAT	0	0	1.00	Limits		11-24
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Input Leak Current	TLI	V _{IN} = 5.25V	TAG	() = n	10	μΑ
Vpp Power Current	Ірр	CE = PGM = VIL	-	-	30	mA
Vcc Power Current	Icc		- 80		150	mA
Input Voltage "H" Level	VIH	— ·	2.0	- 1	Vcc+1	V
Input Voltage "L" Level	VIL		-0.1	-/-	0.8	V
Output Voltage "H" Level	Vон	_	2.4		_	V
Output Voltage "L" Level	VOL		_	-/	0.45	V

AC CHARACTERISTICS

 $(Vcc = 5V\pm5\%, Vpp = 21V\pm0.5V, Ta=25^{\circ}C\sim5^{\circ}C)$

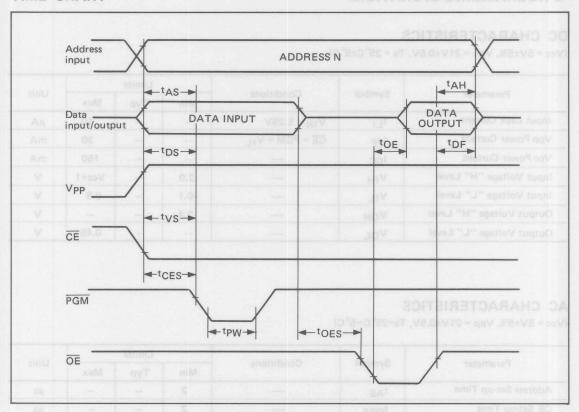
Parameter	Cumbal	Canditions		Limits		Unit
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Address Set-up Time	tAS	_	2	_	_	μs
OE Set-up Time	tOES	_	2	-	-	μs
Data Set-up Time	tDS		2	_	_	μs
Address Hold Time	tAH	_	0	_	-	μs
Data Hold Time	^t DH		2	_	SOHAT	μs
OE Output Valid Delay Time	^t DF		0	_	130	o ans
V _{pp} Power Set-up Time	tvs		2	_	_	μs
Program Pulse Width	tpW	Conditions	45	50	55	ms
CE Set-up Time	tCES	Vo = M <u>tV</u>	2	_	secitance	μs
OE Output Valid Delay Time	tOE	V0 = TUQV	T002_	_	150	ns

Measurement condition

Input pulse level 0.8V \sim 2.2V Input rise/fall time Under 20 ns

Output timing reference level Input 1V, 2V/output 0.8V, 2V

TIME CHART



CAPACITANCE

 $(Ta = 25^{\circ}C, f = 1MHz)$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Input Capacitance	CIN	VIN = 0V	e mod	4	6	pF
Output Capacitance	COUT	VouT = 0V	301	8	12	pF

OKI semiconductor

MSM27128AS

131,072-BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

(E3-S-022-32)

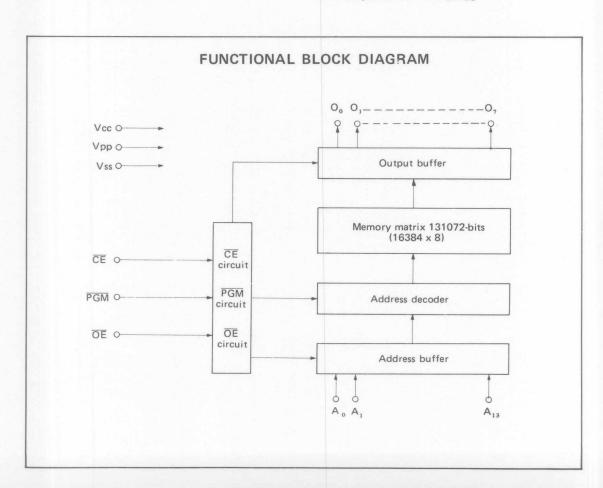
INTRODUCTION

MSM27128AS is a 16384 word x 8-bit read-only memory capable of being erased by ultra violet light. The user may thus generate the desired memory contents, and subsequently alter the contents very simply, making this device ideal for processor programming etc.

MSM27128AS has been manufactured by N-channel silicon gate MOS techniques with a floating gate, and sealed in a standard 28-pin cerdip package.

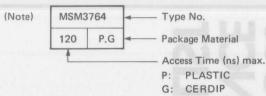
FEATURES

- Single power supply +5V
- Power consumption 788 mW during operation, 184 mW during standby mode
- Ultra violet light erasable, and electrically rewritable
- Reduced programming time. 150 seconds for all 131,072 bits
- Full decoding 16384 words x 8 bits
- Static operation Clock unnecessary
- Input/output TTL connection possible (tristate output)
- Simple expansion of memory capacity (wired OR connections)
- Access time 250 ns
- Pin-compatible with Intel 27128



						R	?[R	EN	1CI
										SIDE	IS
										00	
MK4184-30											





C: SIDE-BRAZED

1. DYNAMIC RAM

truc- ture	Total Bit		Num- ber of Pin	C	Oki	Hit	achi	In	tel	Т	exas	Mo	stek	Mot	torola	N	EC	To	shiba	Mits	ubishi	Fuj	jitsu
								211	7-5					MCM ²	1116-30	μΡΕ	0416						
				1.5				300	P.G					300	G.C	300	P.G					9	
						HM4	716A-4	211	7-4	TMS	1116-25	MK4	1116-4	MCM ²	1116-25	μPD	416-1	TMN	1416-4	M5K	4116-4	MB8	116N
						250	P.G	250	P.G	250	P.G.C	250	P.G	250	G.C	250	P.G	250	G	250	P.G	250	С
				MSM	3716-3	НМ4	716A-3	211	7-3	TMS4	1116-20	MK4	1116-3	MCM4	1116-20	μPD	416-2	TMN	1416-3	M5K	4116-3	MB8	116E
	16k	16384	16	200	С	200	P.G	200	P.G	200	P.G.C	200	P.G	200	G.C	200	P.G	200	G	200	P.G	200	С
	TOK	x 1	10	MSM	3716-2	HM4	716A-2	211	7-2	TMS	1116-15	MK4	116-2	MCM ²	1116-15	μPD	416-3	TMN	1416-2	M5K	4116-2	MB8	116H
				150	С	150	P.G	150	P.G	150	P.G.C	150	P.G	150	G.C	150	P.G	150	G	150	P.G	150	С
						НМ4	716A-1															MB8	216E
						120	P.G															120	С
						НМ	4816		1,4									19 19					
						100	С																
	64k	65536 64k x 1	16																				
				MSM3	764-15	НМ4	864-2	216	4-15	TMS4	1164-15	MK4	164-15	MCM6	664-15	μPD4	1164-3	TMM	4164C-3	M5K4	164-15	MB82	264-1
				150	С	150	С	150	С	150	С	150	С	150	С	150	С	150	С	150	С	150	С
				MSM3	764-20	НМ4	864-3					MK4	164-20	МСМ	6664-20	μPD4	1164-2	TMM4	164C-4	M5K4	164-20	MB82	264-20
				200	С	200	С					200	С	200	С	200	С	150	С	200	С	200	С

Struc- ture	Total Bit	Or- gani- zation	Num- ber of Pin		Oki	Hit	achi	Intel	Т	exas	Мо	stek	Mot	orola	N	EC	Tos	hiba	Mits	ubishi	Fuj	itsu
																			M5K41	64A-10	MB82	264A-10
																			100	P.C	100	P.G
				MSM3	3764A-12	НМ48	364A-1		TMS4	164A-12			MSM66	664A-12	μPD4	164A-4	TMM4	164A-2	M5K41	64A-12	MB826	64A-12
				120	P.C	120	P.G		120	P.C			120	С	120	P.G.C	120	Р	120	P.C	120	P.G
	64k	65536 x 1	16	MSM3	3764A-15	НМ48	364A-2		TMS4	164A-15			мсм6	664A-15	μPD4	164A-3	TMM4	164A-3				
				150	P.C	150	P.G		150	P.C			150	С	150	P.G.C	150	Р				
				MSM3	3764A-29	HM48	364A-3		TMS4	164A-20			мсм6	664A-20	μPD4	164A-2						
		×8		200	P.C	200	P.G		200	P.C			200	С	200	P.G.C						
		2049															100	P = P			100 J	



2. STATIC RAM

Struc- ture	Total Bit	Or- gani- zation	Num- ber of Pin	C)ki	Hi	tachi	In	itel	Т	exas	Mo	ostek	Mo	torola	N	IEC	Tos	hiba	Mitsu	ubishi	Fuj	jitsu
						HM47	72114A			TMS4	1045-15					μPD2	114L-5					MB8	114H
						150	P.G			150	P.G.C					150	P.G					150	P.C
				MSM2	114L-2	HM47	2114A	2114	4/L-2		IS40/ 5-20	MK4	1114-3		M21/ 1-20	μPD2	114L-3	TMM:	314A/	M5 L2	2114L	MB81	114EL
				200	Р	200	Р	200	P.G	200	P.G.C	200	P.C	200	P.C	200	P.G	200	Р	200	P.G	200	P.C
											IS40/ 5-25	MK4	114-4		M21/ 1-25	μPD2	114L-2						
						<u>E</u>				250	P.G.C	250	P.C	250	P.C	250	P.G						
NMOS				MSM2	114L-3	HM47	2114-3	2114	4/L-3			MK4	114-5		M21/ 1-30	μPD2	114L-1			M5L2 -3	2114L	MB81	114NL
	4k	1024	18	300	Р	300	P.G	300	P.G			300	P.C	300	P.C	300	P.G		T-	300	P.G	300	P.C
		× 4		MSM	2114L	HM47	2114-4	211	14/L		IS40/ 5-45				M21/ 1-30	μΡΕ	2114	тммз	14A/L	M5L2	2114L		
				450	Р	450	P.G	450	P.G	450	P.G.C			450	P.C	450	P.G	450	Р	450	P.G		
						L												TMM2	016P-1		4-1	MB	8168
	16k	2048	24															100	Р			100	
	TOK	x 8	24	MSM2	2128-12	200				200				200		200		1					
				120	Р	HME	194A-3			TMS4	164A-20			MCIMB	664A-20	Mp.Dvj	164A-2						

Struc- ture	Total Bit		Num- ber of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Tos	shiba	Mits	ubishi	Fuj	itsu
				MSM2128-15	500 B					200 P	TMM	2016P	5872	25-15	MB8	3168
				150 P	HM6116/L-4					µPD446-2	150	P	150	P.C	150	
		1048 x 8	24	MSM2128-20	150 P					150 8			58	725		
				200 P	HMB116/L-3					16D-646-3			200	P.C		
	y i			MSM5104-2	120 P											
				200 P	4MB116/L-2											
											800-				MB8	404E
											109	514-2			250	Р
COMS		4000		MSM5104-3							650					
OIVIS		4096 x 1	18	300 P							TCBI	144-1				
ios					HM4315				MCM146504	450 8	TC5504		450			
				MSMS114	450 P				450 P.C	PhDett	450	Р	MESS	81-46		Ĭ.
	4K	024 x 4	18		300 6					300 В	TC5	504-1				
				MSM6114-3	HM4334-3					pPD444-1	550	Р				
										250 P	TC5	504-2				
										ThDDddd 5	800	Р				
				MSM5115-2						200 - ь						
				200 P						APDA44-3				×		
		1024									800				MB8	414E
		1024 × 4	18								LCR	843-5			250	Р
		024	18	MSM5115-3							550					
				300 P							1080	19.3-1				



Struc- ture	Total Bit	Or- gani- zation	Num- ber of Pin	0	ki	Hit	achi	Intel	Texas	Mostek	Motorola	N	EC	Tos	hiba	Mitsu	bishi	Fujitsu
				300	Ь									TC5	047-1			
	4k	1024	18											550	Р			
	41	x 4	18											TC5	047-2			250 P
		1												800	Р		4	M88414E
				MSMS	5114-2							μPD	144-3					
				200	P							200	Р					
												μPD	444-2	800				
												250	Р					
				MSMS	5114-3	НМ4	334-3					μPD	444-1		ь			
	4k	1024 x 4	18	300	Р	300	Р					300	Р	1	pos-1			
				MSM	15114	HM4	334-4				450 P.C	μΡΕ	444	TCS	5514	M589	81-45	
CMOS				450	Р	450	Р				MCN146504	450	Р	450	Р	450	G	
		4088												TC5	514-1			
CONS		Shoo		MSM	5104-3									650	Р			
														TC5	514-2			250 P
														800	Р			MBS404E
				MSM5	128-12	HM61	16/L-2											
		11.1		120	P	120	Р											
				MSM5	128-15	HM61	16/L-3					μPD4	146-3			200		
	16k	2048	24	150	P	150	Р					150	Р			188	126	
	TUK	x 8	24	MSM5	128-20	HM61	16/L-4					μPD	146-2	TC5	517-2	180		180
				200	Р	200	Р					200	Р	200	Р	5677	26-16	MB8168
TOTAL			Fin									μPD	446-1	TC5	517			
Sime		Geun	Num ber o			HS	mehi	Intel		Mostek	Wotorola	250	Р	250	Р	Mits		Fultan

Struc- ture	Total Bit	Or- gani- zation	Num- ber of Pin	0	ki	Hit	tachi	Intel	Texas	Most	ek	Motorola	NE	C	Tosh	niba	Mitsu	ıbishi	Fujitsu
				MSM5	127-15				1				μPD4	47-3					
				150	Р								150	Р					
				MSM5	127-20								μPD4	47-2	TC55	16-2			
	ser	- 5		200	Р								200	Р	200	Р			
				7638438									μPD4	47-1	TC5	516			
		5		ј. р			450 P.G						250	Р	250	Р			
				0843684			2364A						μPD	447	23100	364			
												P.C	450	Р			950		
MOS	16k	2048	24	MSM5	129-15	HM61	117/L-3		1.00		N	CW68A	μPD4	49-3			M5M5	118-15	
IVIOS	1011	x 8	300	150	Р	150	Р			5.6		P.C	150	Р			150	Р	
				MSM5	129-20	HM61	117/L-4		MK380	00-2	3(μPD4	49-2			MSM	5118	
				200	Р	200	Р					CMESA	200	Р			200	Р	
					360	B		450 940	300	ts 43	381	1 66	μPD4	49-1					
		× 8				332		TMS4732		60-5		CM58A	250	Р					
	32K ²	1095 2		ь			450 P.G						μPD	449	460	6	150	b 3	Ю ь
				M2932			2332A						450	Р	TMM		MESS:		MB8332
				MSM5	126-20	HM61	I16/L-4		980	P.C	350	P.C	μPD4	46-2	TC55	517-2	880	re	
				200	Р	200	Р			00-0		64	200	Р	200	Р	M587		
	reir .	1048 × 8 - 2		MSM5	126-25							034000A	μPD4	46-1	TC5	517			
		LIVES .		250	P	6	450 P.G			5 C		P.C	250	Р	250	Р			19 6
				SN2916	1414463	318E	2316E		MK34	100-3	N N	CN658A 6A	μPD	446	TMM	334			W88316
		stion P											450	Р					



3. MASK ROM

Struc- ture	Rit		Num- ber of Pin	(Oki	Hit	achi	Inte	el	Те	×as	Mo	stek	Mot	orola		EC	Tos	hiba	Mitsu	ubishi	Fu	jitsu
				MSN	/l2916	HN46	2316E	231	6E			MK34	4000-3	MCN 316/	//68A A		D446	TMI	V1334			МВ	8316
	16k	2048	24	250	Р	450	Р	450	P.G			350	P.C	350	P.C		- b	450	Р			450	Р
	TOK.	× 8				b		1 6				MK31	000-3	MCN 316	//68A	μPD	2316	TMN	1331A	M58	3731		
						28-20		116/L	4			550	P.C	350	P.C	450	P.G	450	81P3	650	P.G		
				MSN	/12932			233	2A							μPD	2332	TMI	M333	M58	3333	МВ	8332
	32k	4096	24	300	Р			450	P.G							450	P.G	450	Р	650	Р	200	Р
	32K	x 8	24			HN4	6332			TMS	4732	MK32	2000-5	MCN 332	/168A								
						350	Р			450	P.G	300	P.G	350	P.C					-			
NMOS				MSI	M2965	58-50	HME	117/1				MK36	6000-5	MCN 364	/168A		449-2			1/4	SME118		
			24	300	P	h	150	1		1.1		300	P.G	250	P.C	150	b			150	ь		
CIVIOS	64k	8192 × 8	24			HN4	3364	117/L	-3					MCN 364	/168A					M58	8334	8	
						350	Р							350	P.C	450				650	Р		
			00	MSN	M3864			236	4A							μPD	2364	TMN	/12364				
			28	250	.Р			450	P.G							450	P.G	250	Р				
	1001		00	MSM	138128											μPD	23128	500	1				
	128k		28	450	P.C	ь										250	С	200					
				MSM:	38128A	03'00											1						
				250	Р	ь																	

CROSS REFERENCE LIST

4. EPROM

Struc- ture	Total Bit		Num- ber of Pin		Ok	i	Hit	achi	Int	tel	Те	xas	Mos	tek	Moto	orola	NE	С	Tosi	hiba	Mitsu	ıbishi	Fuji	tsu
									271	6-1			MK2	716-6	MCN	127A								
									350	С			350	С	350	С								
									271	6-2			MK2	716-7										
									390	С			400	С										
	16k	2048	24	MSM2	2716	cerdip	HN46	62716	27	16			MK2	716-8	МСМ	2716	μPD2	716	TMN	1323	M5L	2716	MB8	516
		x 8		450)	С	450	С	450	С			450	С	450	С	450	С	450	С	450	С	450	С
																					M5L2	716-65		
																	-				650	С		
											TMS	2516												, T
MOS											450	G.C							2.1					
VIVIOS	V.					4-20AS			276	4-2									TMM2	764D-2	M5L27	764K-2	MBM27	64-20
	64k	8192	20		200 ER[-				_				200	С	200	С	200	С
	04K	x 8	28			4-25AS		32764	27	64							μPD2	764	TMM2	2764D	M5L2	764K	MBM2	64-25
					250 ERI			Ons C					-						250	С	250	С	250	С
						4-30AS			276	4-3											M5L2	764K-3	MBM2	64-30
					300 ERI			00n C													300	С	300	С

M

MONAGE OF

APPLICATIONS

MEMORY DRIVER

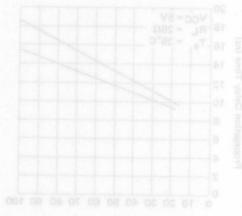
here are problems in driving MOS ICs by a TTL driver: icrease of driver delay time due to capacitive load and inding waveform at the falling edge.

in example of the Increase of delay time due to capacive toud is shown in the following figure.

he number of load mentory elements must be taken

gyr 2.1 to reso r

ROPAGATION DELAY TIME



CL - Load Capacitance - PF

• If the number of load memory elements is 20 - 40 (150 - 300F) on a two layer board, an undershoot of -2 to -3V (peak voltage) occurs. Therefore, mass uses against maging must be taken as described in the following

Measures assinst ringing

- No consideration is required for the rising adgaaince there is a mergin.
- Since a ringing may be considered as a reflection due to mismatching between the driver output impedance and signal line impedance, it can be prevented by telding the line matching (termine sized).

For memory arrays, however, termination with pull up or bleeder resistance is not effective instead, series resistance (damping resistance) is suitable for memory arrays.

- The optimal value of series resistance differ depending upon the speed, pertern status, and driver, Experiences will help much in determinity the optimal series resistance.
- As a standard, a resistance of 10 ~ 100.0 is suitable.

Note that the speed will be lowered if the relief ence is so great. An example is shown in atteched drawled 3.

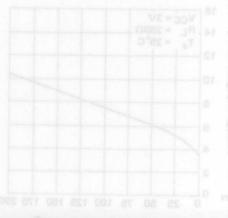
(d) Make the signal lines as short as possible. Multilayer board design is effective in reducing the undershoot less the signal line impedence. It towered?.

agent I have a

S112, S114 S114

AVERAGE PROPAGATION DELAY TIME
CLOCK TO OUTPUT

LOAD CAPACITANCE



64K BIT DYNAMIC RAM APPLICATION NOTES

1. MEMORY DRIVER

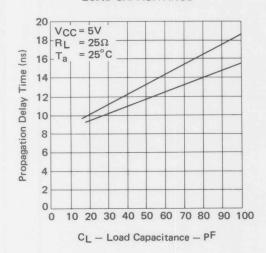
There are problems in driving MOS ICs by a TTL driver: increase of driver delay time due to capacitive load and ringing waveform at the falling edge.

An example of the increase of delay time due to capacitive load is shown in the following figure.

The number of load memory elements must be taken into consideration when designing the timing.

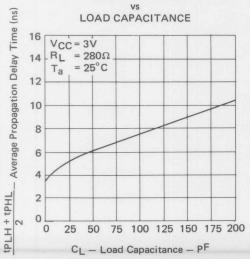
In case of LS type

PROPAGATION DELAY TIME vs LOAD CAPACITANCE



In case of L type

'S112, 'S113, 'S114 AVERAGE PROPAGATION DELAY TIME CLOCK TO OUTPUT



• If the number of load memory elements is $20 \sim 40$ (150 $\sim 300 \text{PF}$) on a two layer board, an undershoot of -2 to -3V (peak voltage) occurs. Therefore, measures against ringing must be taken as described in the following.

Measures against ringing

- No consideration is required for the rising edge since there is a margin.
- (2) Since a ringing may be considered as a reflection due to mismatching between the driver output impedance and signal line impedance, it can be prevented by taking the line matching (termination).

For memory arrays, however, termination with pull up or bleeder resistance is not effective. Instead, series resistance (damping resistance) is suitable for memory arrays.

(3) The optimul value of series resistance differs depending upon the speed, pattern status, and driver. Experiences will help much in determining the optimul series resistance.

As a standard, a resistance of $10 \sim 100 \Omega$ is suitable.

Note that the speed will be lowered if the resistance is so great. An example is shown in attached drawing 3.

(4) Make the signal lines as short as possible. Multilayer board design is effective in reducing the undershoot (as the signal line impedance is lowered).

2. DECOUPLING CAPACITORS

The dynamic MOS RAM is featured by the great power current at the active time in comparison to that at the standby time.

For example, the rated value (Icc1) of the mean power current of the MSM3764 is 45mA, while the standby current (Icc2) of the MSM3764-15 (150ns version) is 5mA. The former is approximately 10 times greater than the latter. The peak current of the MSM3764 approaches 90mA in the worst case. It is approximately 20 times as great as the standby current Icc2.

Therefore, the power circuit must be designed so as to prevent the above current variation from causing an erroneous operation of the memory. A by-pass capacitor must be inserted for this purpose. There are two types of by-pass capacitors: high frequency capacitor and low frequency capacitor.

2.1 High Frequency Capacitor

In the lcc current waveform, the peak current rises at a high speed such as 10ns, and a high frequency noise represented by the following expression is caused to occur by the L component of the current applied to the capacitor:

$$\triangle V = L \frac{\triangle i}{\triangle t}$$

To reduce the fluctuation $\triangle V$, the value of L must be reduced.

For this purpose, the capacitor must be placed as close as possible to the power pin of the IC. Further, sufficient capacity for supplying the peak current is required. The standard capacity for a double sided circuit board (two layer circuit board) is $0.05 \sim 0.1 \mu F$ or more. The capacity may be less than this value for a multi layer circuit board since the L component is less than the former.

When designing a board, mount one capacitor with excellent high frequency characteristics for every two or three MOS IC memory chips, near the power pins of these IC chips.

2.2 Low Frequency Capacitor

A low frequency capacitor is required for suppressing the power fluctuation due to a sudden current variation (for example, current variation caused by a status change from the standby status to the continuous access status or concurrent refreshment of the entire board) in a board unit. The power fluctuation in this case is a slow variation of several handred ns.

For this reason, the low frequency capacitor must have a capacity larger than the high frequency capacitor.

Though the capacity requirement depends upon the number of memories which operate simultaneously (bit width), $50\mu F$ is enough for a $16 \sim$

32 bit system in a practical use.

As an example of capacitor which satisfies the requirements in both 2.1 and 2.2 above, a small-sized tantalum capacitor with excellent high frequency characteristics is shown in the following table. It is desirable to mount a low frequency capacitor near the power input pin in order to suppress the fluctuation of power supplied from outside, even if this capacitor is mounted.

Manufacturer	Model	Capacity (µF)
Oki Ceramic Co.	Model CA	0.1 - 20.5
	tantalum capacitor Model CB	0.1 ~ 20μF

The frequency characteristics of the above capacitor and the power bus bar are illustrated in attached figure 1.

3. PRINTED CIRCUIT BOARD

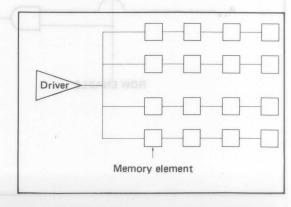
3.1 Number of Layers

Considering the measures against power noise which was described in 2. above and the routing to be described in 3.2, two layers are enough in principle.

3.2 Routing

An example of routing on a two-layer circuit board is shown in attached drawing 2. In designing the routing, note the following four points:

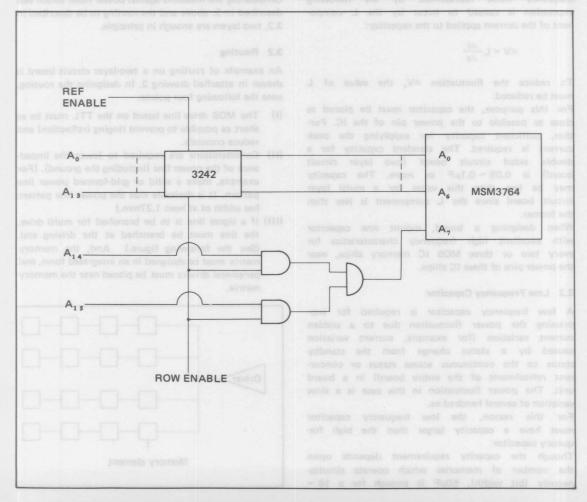
- The MOS drive line based on the TTL must be as short as possible to prevent ringing (reflection) and reduce crosstalk.
- (II) Considerations are required to lower the impedance of the power line (including the ground). (For example, make a solid or grid-formed power line pattern. It is desirable that the power line pattern has width of at least 1.27mm.)
- (III) If a signal line is to be branched for multi drive, the line must be branched at the driving end. (See the following figure.) And, the memory matrix must be designed in an integrated form, and peripheral drivers must be placed near the memory matrix.



4. PERIPHERAL CONTROL CIRCUIT

The three types of dynamic RAM control ICs shown in the following table are available at present.

Manufacturer	Model	Functions
Intel	i-3242	Seven-bit address multiplexer (for 16K bit dynamic RAM) Seven-bit refresh address count function
Motorola AO Isbail	MC-3242	 Direct dirving capability of memory elements (for approx. 20 elements. 250 pF/25 ns 15 pF/9 ns) Application to a 64K bit dynamic RAM, example (see the following figure)
Texas Instruments (T. I)	74LS601 603	 Refresh timer using an RC multivibrator Timing generation Refresh address (7-bit address)
Advanced Micro Device (AMD)	Am2964A	 ○ Address latch/multiplex function (16-bit address) ○ Refresh address counter ○ RAS decoder (2 ~ 4)
Intel	i-8203	8-bit address multiplexer (for 16K/64K DRAM) Direct dring capability of memory element Including timing control



5. NOTES ON MOUNTING 1 MB MEMORY ON A BOARD

The advent of a 64K bit dynamic RAM such as the MSM3764 has made it extremely easy to mount 1 MB

memory on a board from the viewpoint of mounting space. In this case, however, note the following points since the number of memory elements mounted is so large as $128 \sim 176$ (when redundant bits are provided).

Point to be noted	Consideration	Practical example				
Mounting of memory elements	Memory elements may be integrated or divided. (Design the memory array(s) to make the drive lines shortest.)	Driver		Memory		
ddress capacity. The ty is expressed a cror rate!	the drive lines shortest.	Memory arr	Driver ay Memo	ory arra	ilidelle se tiet y	
Memory Take care about the delay time and		Drive element	Logic et Memory	ysteides	07 E7 VI	
element driving method	undershoot noise of the drive element. (If the condition V _{ILmin} = -1V recommended for the MOS dynamic RAM operation is satisfied, the memory elements	Parameter Element	Delay time	(mA) IOL	Noise	
	will display the full reliability.)	7404	Medium speed	16	0	
n without bit corre		74S04	High .	20	×	
Measures against noise	 Two layers are enough for a board. (Pay attention to the power line pattern.) 	or that does not reg a for soft errors:	time cause	or is a round and sent the	ns The phiwol	
	High frequency noise	Mount a 0.1 \sim 1 μ F capacitor for every to memory elements.				
	Low frequency noise	Mount a tantalum capacitor etc. of 50 μ or more near the power input pin of the memory package.				
Timing design	Prevent skew between each timing in order to enhance the system access speed.	Use ICs of the same tipe for racing ti (for example, RAS or CAS).		timing		
128k byte, and 256	Make a sufficient margin in timing design.	Skew and mounting delay			in a	
Thermal design	Thermal design under the worst condition is required.	Operation at a case temperature of 70 must be guaranteed.			70°C	

6. MEMORY SYSTEM RELIABILITY

6.1 Reliability Determination Factors

The memory system reliability depends upon the four factors shown in the left column of the following table. These factors are determined as shown in the right column of this table.

Memory system reliability factor	Factor determination		
System-required reliability	Determined by the user-required specifications (MTBF).		
Unit capacity	α [MB] = [word depth] x [bit count]		
Parts reliability	Logic element — Hard error Memory element — Soft error		
Cost	Parameter Delay		

6.2 Hard Error and Soft Error

(I) Hard error

A hard error is a permanent error which occurs each time a certain address is accessed.

(II) Soft error

A soft error is a transient error that does not repeat. The following are the three causes for soft errors:

- (1) Insufficient power margin
- (2) Insufficient system noise margin
- (3) Particle failure
- (4) Insufficient power margin
- (5) Insufficient system noise margin
- (6) particle failure

Items (1) through (5) are largely influenced by the system design. For item (6), it is required to consider whether a remedy such as ECC should be taken or not to satisfy the system-required reliability based on the parts reliability (pertaining to hard errors and soft errors). See 1.3 and 1.4 for details.

6.3 Measures for Reliability Enhancement

The following are the two typical means for the enhancement of system reliability.

- (1) Parity...... Error detection only (makes no contribution to the MTBF enhancement)
- (2) ECC..... The SEC-DED* is used in general

* <u>Single Error Correct</u> — <u>Double Error Detect</u> (one bit error correction and two bit error detection)

6.4 Reliability Calculation Method

MTBF for a hard error and a soft error

(1) Memory element reliability

Hard error $r_H = e^{-\lambda H \cdot t} (\lambda_H)$: Hard error rate) Soft error $r_S = e^{-\lambda S \cdot t} (\lambda_S)$: Soft error rate) Reliability

$$R = \underbrace{(r_H)}_{\text{(1)}}^n + \underbrace{nC_1 \cdot (r_H \cdot r_S)^{n-1} \cdot (1 - r_H)}_{\text{(2)}}$$

- 1 Probability of no hard error
- Probability of one bit hard error followed by no hard or soft error

Find a value for t when the value of R is e⁻¹

The following calculations are based on the assumption that there is a low probability of two bit soft error occurrence.

(2) Memory unit reliability

Assume a memory unit whose size is n bits in bit width and k blocks in address capacity. The memory element reliability is expressed as follows:

$$r = e^{-\lambda t}$$
 (λ : error rate)

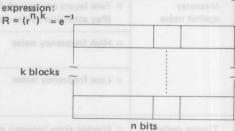
1) One bit correction

Find a value for t which satisfies the following expression:

$$R = \{ (r)^{n} + nC_{1} \cdot r^{n-1} (1-r) \}^{k} = e^{-1}$$

- 1 Probability of all bits being correct
- Probability of error occurrence for only one bit
- Only parity error detection without bit correction

Find a value for t which satisfies the following expression:



6.5 Reliability Calculation Result Example

- (1) Comparison of 64k byte, 128k byte, and 256k byte configurations (without ECC)
 - 1) 64kbyte

Element	λΗ (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	11.5
		200	10.6
	50	100	15.9
101		50	21.1
16k		200	12.7
7 4		100	21.1
		50	31.7

② 128kbyte

Element	λΗ (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	5.8
		200	5.3
по	100	100	7.9
101		50	10.6
16k	ted drive :	200	6.3
ist be stric	50	100	10.6
peak ditte		50	15.9
the same than the same of the same of			

3 256kbyte

			_
Element	λΗ (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	2.9
		200	2.6
al item to be	100	100	4.0
101		50	5.3
16k		200	3.2
	50	100	5.3
		50	7.9

Notes: 1. The bit width is 9 bits for each case.

2. 1 bit is used for parity error detection.

(2) Comparison of 1M byte configurations (with ECC)

Element	NU (E:+)	λS (Fit)	Reliabilit	y (years)
Element	λΗ (Fit) λS (Fit)		Bit width: 22 bits	Bit width: 39 bits
64k	100 (100%)	1000	8.2 (0.76)	7.9 (0.79)
lu0.1 mulstras	100 (50% 50%)	1000	13.9 (0.76)	14.5 (0.79)
(Seramia)	100 (100%)	100	8.3 (1.05)	6.8 (1.08)
16k	100 (50% 50%)	100	13.0 (1.05)	10.7 (1.08)

Notes: 1. When the bit width is 22 bits, six bits are used for the ECC.

- When the bit width is 39 bits, seven bits are used for the ECC.
 - Values in parentheses are the reliabilities in the case of parity error detection without ECC.
- 4. The (50%, 50%) in the λH column means that 50% of the hard error rate λH is handled as the total bit hard error rate and the remaining 50% is handled as the one bit hard error rate (which reflects the hard error mode analysis result confirmed so far).

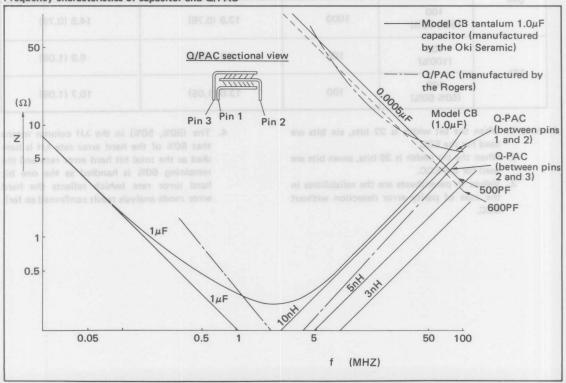
MEMORY COMPARISON STANDARD

In general, power, speed, and usability are required for memory elements. At present, 64K bit dynamic RAMs can be supplied by a lot of manufacturers, and these elements have almost unified specifications. In designing a circuit board to achieve stable system operation, however, considerations must be given to the specification values and margins against the specification values, pertaining to the points shown in the following table. Factors that will affect the stable system operation are power, temperature, aging, clock skew, uneven operation of peripheral ICs, and so forth.

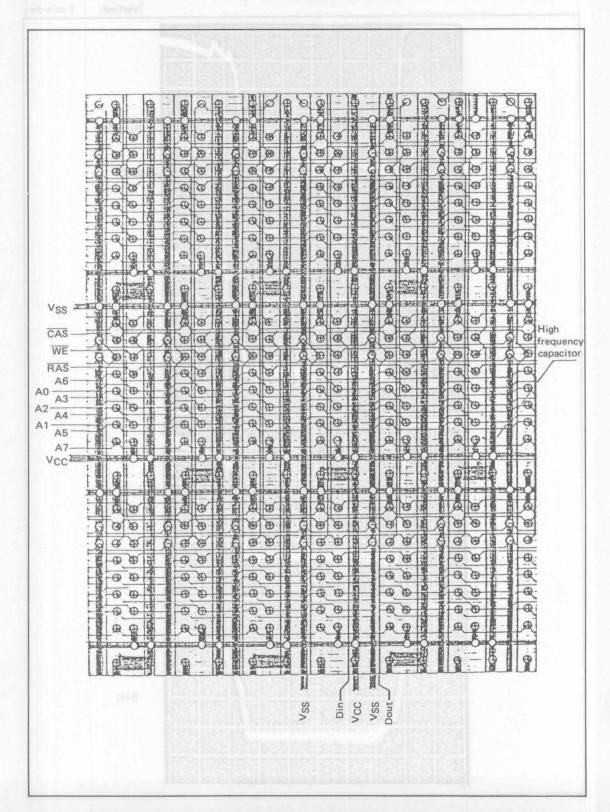
Point to be noted	00	Actual item to be considered	Reason
Power	00	Currents (Icc1, Icc3, and Icc4) at the operating time and current (Icc2) at the standby time	The power system must be noted. (example: with battery backup)
6.3	00	Current waveform (especially the peak current value)	The noise margin must be strict for memories with large peak current.
Timing margin	2010	 Address setup (t_{ASR}, t_{ASC}) and hold (t_{RAH}, t_{CAH}) timing 	In system designing, these timing pulses are directly related to the access time.
	yair	Data setup (tDS) timing and write pulse width (tWP)	These timing pulses are related to the cycle time in writing.
		Voltage, temperature, and dependability of each timing (especially the tREF and tRAC)	The temperature inclination must be little for the timing pulses tREF and tRAC.
Voltage margin	blw	It is impossible to achieve the ideal voltage status when used within a system.	A sufficient voltage margin must be provided under consideration of various factors which will affect the system operation stability.

Attached drawing 1

Frequency characteristics of capacitor and Q/PAC

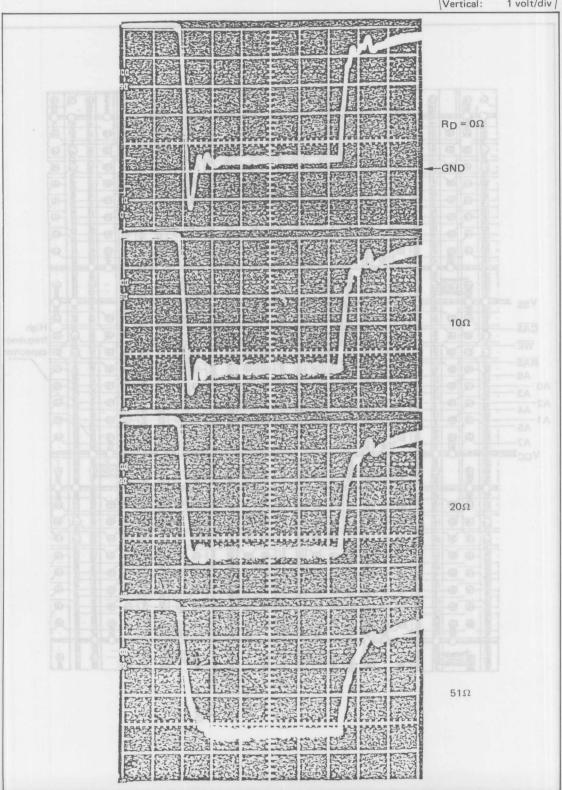


Attached drawing 2
Two layer board circuit pattern example



Attached drawing 3
Input waveform example

Horizontal: 50 ns/div Vertical: 1 volt/div



CMOS RAM BATTERY BACK-UP

A practical example of formation of non-volatile data by CMOS static RAM battery back-up is outlined below.

System power and battery switching circuit

The most simplest RAM power supply (CMOS Vcc) is outlined in Fig. 1. In this case, the CMOS Vcc for normal operation is kept at a voltage 0.7V below the system voltage by the voltage drop across a diode (forward direction).

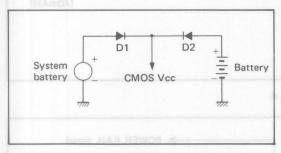


Fig. 1

Fig. 2 is an example of use of a chargeable Ni-Ca battery as the back-up battery. While the system power is being employed, the Ni-Ca battery is gradually charged up via Rc. As in Fig. 1, the diode voltage drop also poses a problem in this circuit.

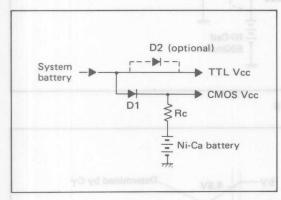


Fig. 2

The conditions for formation of non-volatile data (data retention) by battery back-up are listed below.

- The input signal H level must not exceed Vcc + 0.3V when the CMOS RAM Vcc power voltage is dropped.
- (2) CE (or CS) must maintain CMOS Vcc "H" level.
- (3) In order to minimize power consumption, WE, AD, DIN (or I/O) must be set to GND level or to the same "H" level as CMOS Vcc. (This is not necessary, however, for CMOS RAMs with chip select floating capability).

Note: CS floating capability

Power down possible irrespective of other input levels when memory has not been selected (i.e. when $\overline{CS} = H$).

Consequently, if the TTL Vcc level is greater than the CMOS RAM supply voltage, and the RAM driver is at the TTL Vcc level, the CMOS RAM input voltage will exceed CMOS Vcc + 0.3V (a situation which must be avoided). Therefore, in order to reduce the voltage difference between CMOS Vcc and TTL Vcc with the battery voltage set to at least 4.5V or 4.75V (due to the RAM operating supply voltage range), the D2 diode may be added to abtain a system voltage level at least 0.7V above 4.5 $^{\sim}$ 4.75V (which will keep CMOS Vcc and TTL Vcc within the respective CMOS and TTL operating supply voltage ranges).

To cope with (1) and (3), a CMOS driver which will also operate at a low voltage Vcc during data hold may be employed, or else, the open collector and open drain buffer may be pulled up to CMOS Vcc in order to drive the RAM.

A control circuit for coping with (2) when an abnormal system power supply is detected is also required.

2. Switching Circuit Modifications

Modification of the diode switching circuit can employ PNP transistors. Voltage drops by PNP transistor V_{CE} are smaller by about 0.2V, and this can lead to the generation of a system "power fail" signal.

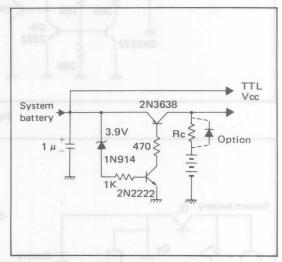


Fig. 3

Fig. 3 outlines a switching circuit employing a PNP transistor. The Rc used when a chargeable battery is employed is replaced by a diode when a non-chargeable battery is used. In this case, switching occurs at the zener diode voltage, so "power fail" must be detected by another circuit, and $\overline{\text{CE}}$ set to CMOS Vcc "high" level.

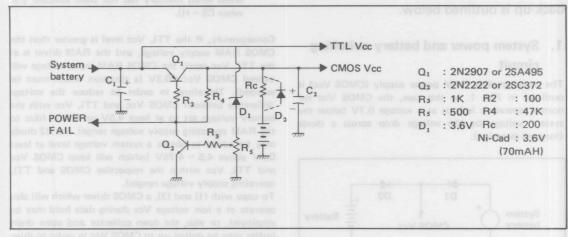


Fig. 4

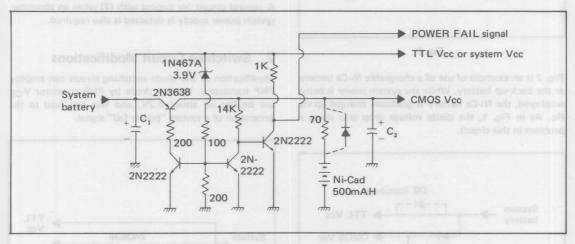


Fig. 5

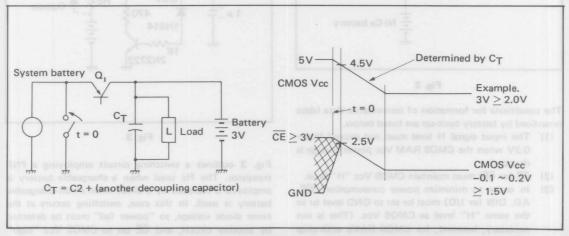


Fig. 6

3. Data Retention Mode

The RAM driver (peripheral circuit) is determined according to conditions (1) and (3) required for data retention. In Oki Electric CMOS RAMs, the power voltage during data retention is kept at a minimum of 2.0V. The $\overline{\text{CE}}$ (or $\overline{\text{CS}}$) voltage at this time has to be kept at about Vcc -0.2V. And as was mentioned earlier, the CMOS Vcc must drop smoothly when the system power

is cut until it reaches the power voltage for data retention (practically equivalent to the battery voltage, or else reduced by the diode voltage drop). And although $\overline{\text{CE}}$ traces the slope of CMOS Vcc reduction at this time, a smooth change in $\overline{\text{CE}}$ is also a necessary condition for actual circuits.

(4) When switching to retention mode, or from retention mode to operation mode, \overline{CE} must exhibit a smooth change. If noise is generated in \overline{CE} in this case, the data will be subject to rewriting.

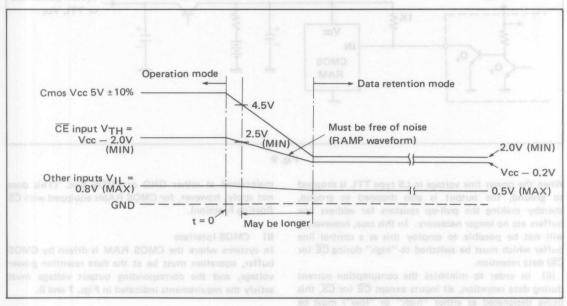


Fig. 7

(5) When switching to operation mode, commence operation after elapse of tRC (read cycle time) following

Vcc reaching the operating power voltage range.

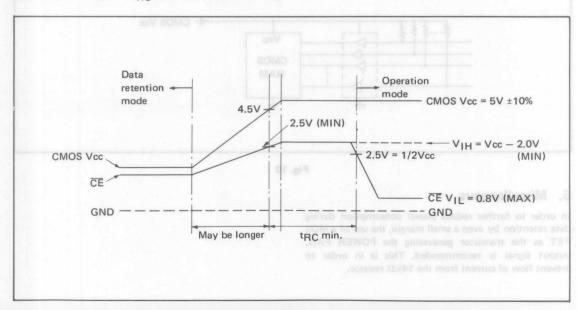


Fig. 8

4. Interfacing

A) TTL Interface

In the case of CMOS RAM drive by TTL, use an open-collector type TTL according to conditions (1) and (3).

When the system power line (i.e. TTL Vcc) is cut, the open-collector TTL Q2 in Fig. 9 is turned off, followed by Q1 also being turned off, resulting in the CMOS RAM input being pulled-up to CMOS Vcc.

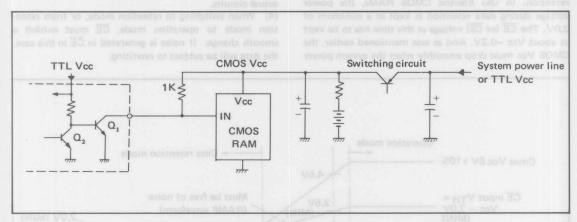


Fig. 9

When the power line voltage in LS type TTL is dropped to ground, the output is also dropped to ground, thereby making the pull-up resistors for address line buffers etc no longer necessary. In this case, however, it will not be possible to employ this as a control line buffer which must be switched to "high" during $\overline{\text{CE}}$ (or $\overline{\text{CS}}$) data retention.

(6) In order to minimize the consumption current during data retention, all inputs except \overline{CE} (or \overline{CS} , this being designated as either "high" or "low") must be

maintained at either GND or CMOS Vcc. (This does not apply, however, for CMOS RAMs equipped with $\overline{\text{CS}}$ floating function).

B) CMOS Interface

In systems where the CMOS RAM is driven by CMOS buffer, operation must be at the data retention power voltage, and the corresponding output voltage must satisfy the requirements indicated in Figs. 7 and 8.

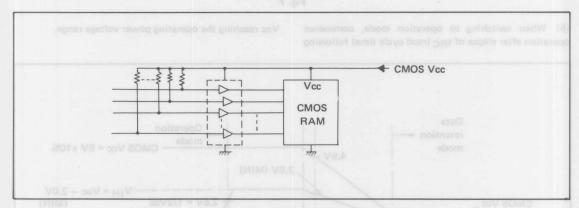


Fig. 10

5. Miscellaneous

In order to further reduce power consumption during data retention by even a small margin, the use of a MOS FET as the transistor generating the POWER FAIL output signal is recommended. This is in order to prevent flow of current from the $14k\Omega$ resistor.



MASK ROM KANJI GENERATION MEMORY DESCRIPTION

1. KANJI GENERATION MEMORIES

	IC models	Number of codes	Character storing capacity	Config- uration	Character style	Bit capacity	Access time
High speed memories	M S M38128- 00 M S M38128- 17	18	JIS standard No. 1 3418 characters	24 × 24	Ming style	128K bits	450μs max
	M S M38128- 18	10	JIS standard No. 1 3418 characters	16 x 18	Gothic style	128K bits	450μs max
Low speed memories	M S M28101A	penerlo ribe bloe outr to	JIS standard No. 1 3418 characters	16 x 18	Gothic style	1M bits	10μs max (16 x 18 transfer)
	M S M28201A	1	JIS standard No. 2 3384 characters	16 x 18	Gothic style	1M bits	10μs max (16 x 18 transfer)

2. MSM38128 SERIES

The electrical specifications of the MSM38128 series high speed kanji generation memory ICs conform to the specifications of the MSM38128 16384 word x 8 bit mask ROM, except that the output enable (\overline{OE}) signal is active when set at a low level. The character data is represented by high level output and background data

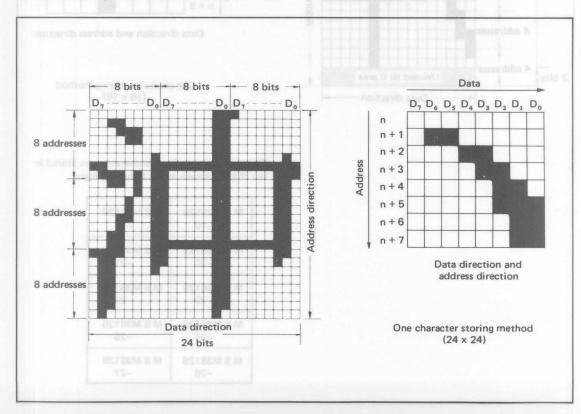
is represented by low level output.

2.1 Pattern Storing Method

(1) 24 x 24 Ming style

The 8 address x 8 bit data per character is stored in one chip, and one character is configured with

nine chips



No. 1 characters are divided into two for storing in two groups of nine chips.

The nine codes to form a character are stored in nine chips as shown in the following figure.

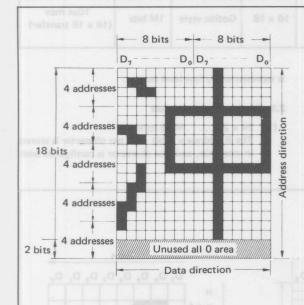
3500	7128980 1 110	HE HOUSE
M S M38128	M S M38128	M S M38128
-00	-01	-02
M S M38128	M S M38128	M S M38128
-03	-04	-05
M S M38128	M S M38128	M S M38128
-06	-07	-08

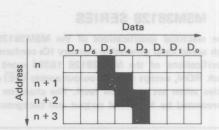
-09	-10	-11	
M S M38128	M S M38128	M S M38128	
-12	-13	-14	
M S M38128 -15	M S M38128 -16	M S M38128 -17	

Correspondence of chips to nine codes of a character

(2) 16 x 18 Gothic style

The 4 address x 8 bit data per character is stored in one chip, and one character is configured with ten chips. Each character data is associated with unused data of two addresses.





Data direction and address direction

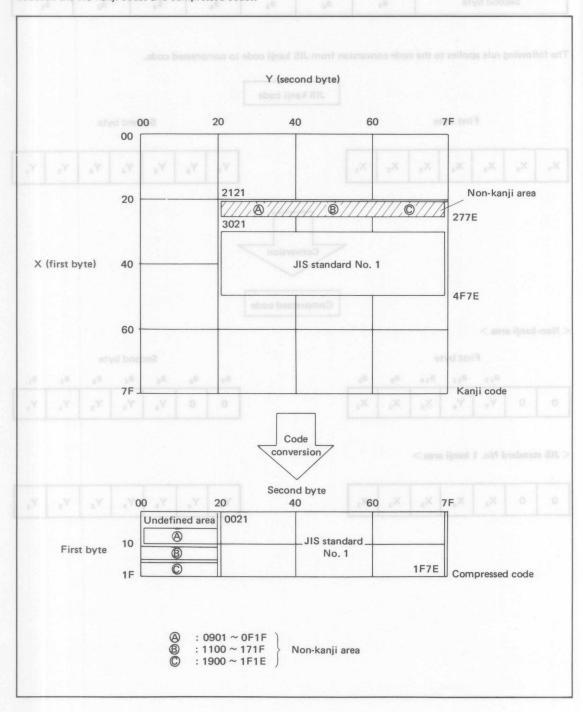
One character storing method (16 x 18)

The ten codes to form a character are stored in ten chips as shown in the following figure.

M S M38128	M S M38128
-18	-19
M S M38128	M S M38128
-20	-21
M S M38128	M S M38128
-22	-23
M S M38128	M S M38128
-24	-25
M S M38128	M S M38128
-26	-27

2.2 Code Compression

The MSM38128 series memories perform code compression so that a correspondence can be established between the JIS kanji codes and compressed codes.



Note: In the case of 24 x 24 character data, the part above the broken line is stored in the MSM38128-00 to 08 chips and the part under the broken line is stored in the MSM38128-09 to 17 chips.

■ MASK ROM KANJI GENERATION MEMORY DESCRIPTION ■

< Compressed code >

First byte	0	0	a ₁₂	a ₁₁	a ₁₀	a ₉	a ₈
Second byte	a ₇	a ₆	a ₅	a ₄	a ₃	a ₂	a

The following rule applies to the code conversion from JIS kanji code to compressed code.

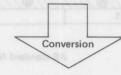
JIS kanji code

First byte

Second byte







Compressed code

< Non-kanji area >

0

First byte

	a ₁₂	a ₁₁	a ₁₀	a ₉	a ₈
0	Y	Y ₆	X ₃	X ₂	X ₁

Second byte

a ₇	a ₆	a ₅	a ₄	a ₃	a ₂	a ₁
0	0	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁

< JIS standard No. 1 kanji area >

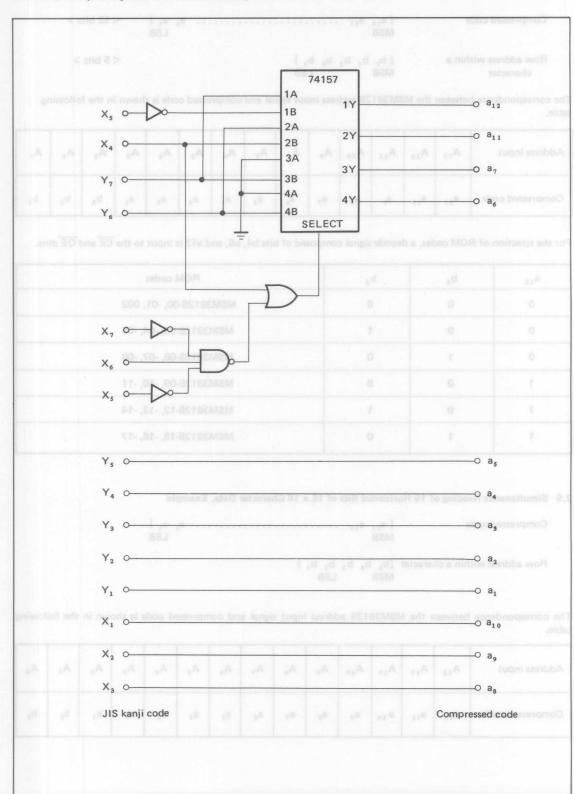


Y₇ | Y₆ | Y₅ | Y₄ | Y₃ | Y₂ | Y₁

11

above the broken line is stored in the MSM38128-00 to 08 chips and the part under the broken line is stored in the MSM38128-09 to 17 chips.

2.3 Code Compressing Conversion Circuit Example and AS at AS to said temperature AS to publish A successful and AS



Row address within a character

[b₅ b₄ b₃ b₂ b₁] MSB LSB < 5 bits >

The correspondence between the MSM38128 address input signal and compressed code is shown in the following table.

Address input	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A _o
Compressed code	a ₁₁	a ₁₀	a ₉	a ₈	a ₇	a ₆	a _s	a ₄	a ₃	a ₂	a ₁	b ₃	b ₂	b ₁

For the selection of ROM codes, a decode signal composed of bits b4, b5, and a12 is input to the CE and OE pins.

a ₁₂	b ₅	b ₄	ROM codes
0	0	0	MSM38128-00, -01, 002
0	0	1	MSM38128-03, -04, -05
0	1	0	MSM38128-06, -07, -08
1	0	0	MSM38128-09, -10, -11
1	0	1	MSM38128-12, -13, -14
1	1	0	MSM38128-15, -16, -17

2.5 Simultaneous Reading of 16 Horizontal Bits of 16 x 18 Character Data, Example

Row address within a character $\begin{bmatrix} \mathbf{b}_5 & \mathbf{b}_4 & \mathbf{b}_3 & \mathbf{b}_2 & \mathbf{b}_1 \end{bmatrix}$ MSB LSB

The correspondence between the MSM38128 address input signal and compressed code is shown in the following table.

Address input	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
Compressed code	a ₁₂	a ₁₁	a ₁₀	a ₉	a ₈	a ₇	a ₆	a _s	a ₄	a ₃	a ₂	a ₁	b ₂	b ₁

■ MASK ROM KANJI GENERATION MEMORY DESCRIPTION

For the selection of ROM codes, a decode signal composed of bits b_3 , b_4 , and b_5 is input to the \overline{CE} and \overline{OE} pins.

b ₅	b ₄	b ₃	ROM codes
0	0	0	MSM38128-18, -19
0	0	1	MSM38128-20, -21
0	1	0	MSM38128-22, -23
0	1	1	MSM38128-24, -25
1	0	0	MSM38128-26, -27

III MASK ROM KANJI GENERATION MEMORY DESCRIPTION III

For the selection of ROM codes, a decode signal composed of birs by, by, and by is input to the CE and OE pins.